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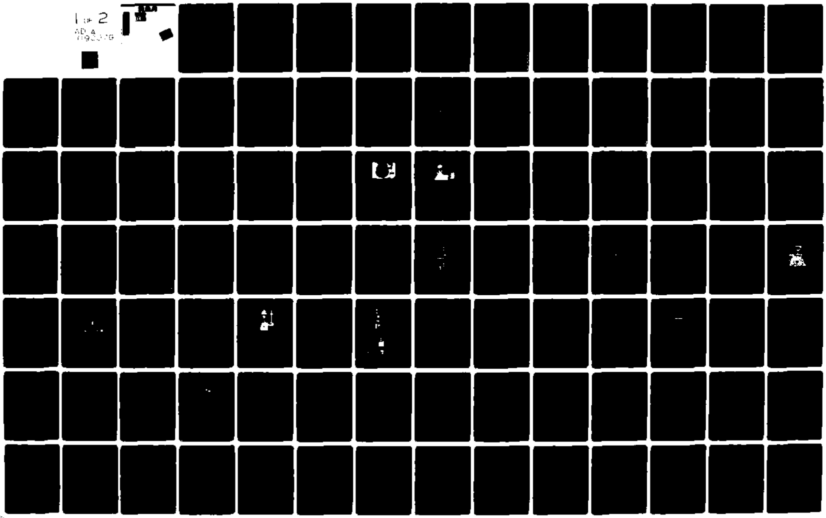

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

RCA has successfully completed the production engineering, fabrication and testing of the five engineering sample devices under this MM&T contract. This report thoroughly describes and discusses the assembly and process procedures as well as the test circuits and test results. Environmental capabilities of the device were verified. The report also includes numerous detailed drawings and graphs to further illustrate the characteristics of this large silicon NPN Transcalent transistor.

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MANUFACTURING METHODS AND TECHNOLOGY (MM&T) MEASURE FOR FABRICATION OF SILICON TRANSCALENT TRANSISTOR

Final Technical Report

Period Covered: 2 April 1979 to 31 March 1980

Object of Study: The objective of this manufacturing methods and technology measure is to establish the technology and capability needed to fabricate Silicon Transcalent Transistors.

Contract No. DAAK70-79-C-0019

Prepared by:
M. F. DeVito
S. W. Kessler
R. E. Reed
D. R. Trout

SUMMARY

This report describes in detail the more important steps in the refinement of the design of the J15381 Transcalent transistor; assembly and process procedures; characteristics inspection test circuits and test results; as well as the preparation of the drawing package. Each of these topics is discussed from a production engineering viewpoint, particularly, as accomplished during the successful fabrication and testing of the five Engineering Sample Devices which have been shipped to the government ahead of schedule in fulfillment of this phase of the contract. The PERT chart, dated 27 April 1979, was used for the scheduling of the various tasks.

At the completion of the Engineering Phase of the Contract, RCA decided to withdraw from the Transcalent Solid State business and therefore requested a modification to the Contract. This report describes additional work done during this phase out period and includes pertinent comments and suggestions pertaining to the manufacture and operation of the transistor.

Table 1 summarizes the characteristics achieved during the engineering phase of the contract.

TABLE 1

SUMMARY OF TRANSISTOR CHARACTERISTICS

Type No. J15381

Electrical Characteristics	Symbol	Min.	Typical	Max.	Units
Breakdown Voltage, Collector to Base	V_{CBO}	750			Volts
Sustaining Voltage	V_{CEO}(sus)	350			Volts
Breakdown Voltage, Emitter to Base	V_{EBO}	8			Volts
Collector Current	I_C(CW)	50			Amps
	i_C(Pulsed)	100			Amps
Forward Current Transfer Ratio, (i_C = 10)	h_{FE} (Pulsed or CW)	20			Times
Saturation Voltage, (i_C = 50 A)	V_{CE}(sat)		0.8		Volts
Thermal Characteristics					
Dissipation (875 LFM, 25°C Air)	P_T	400			Watts
Thermal Impedance, Junction to Case	$R_{\theta jc}$			0.2	$^{\circ}$C/Watt
Case Temperature, Operating	T_C			125	$^{\circ}$C
Case Temperature, Non-Operating	T_C	-55		200	$^{\circ}$C

TABLE 1 (Cont.)

	Symbol	Min.	Typical	Max.	Units
Mechanical Characteristics					
Length (Overall)				See Fig. 1	Inches
Diameter				See Fig. 1	Inches
Weight			12		Oz.
Environmental Characteristics	**Mil/Std/Method**				
Shock, 1 Millisec. Duration	750B/2016.2	500			G
Vibration, 100 to 1000 Hz	750B/2056	5			G
Salt Atmosphere	750B/1041.1	24			Hours
Moisture Resistance, 25°C to 65°C Cycle	202E/106D	10			Cycles
Temperature Cycling, -25°C to 125°C	202E/107D	5			Cycles
Thermal Fatigue Cycling, 30°C to 90°C	--	200			Cycles
Altitude, Corona Free, V_{CEV} = 750 V	750/1001.1	85,000			Feet
Life Test, T_C = 125°C, V_{CE} = 300 V	--	200			Hours

PREFACE

MERADCOM Contract No. DAAK70-79-C-0019, dated 2 April 1979, Project No. A331/E88/79, authorizes the performance of a Manufacturing Methods and Technology (MM&T) measure for the Transcalent transistor, type No. J15381. The contractor is to furnish all personnel engineering, labor, tools, facilities, equipment, materials, supplies and services necessary to perform the work.

The J15381 power transistor was developed originally under MERADCOM R&D Contract No. DAAK02-72-C-0642[1]. This transistor design combines high current at a reasonable gain with high breakdown voltage and superior dissipation capabilities.

The work under the MM&T contract is being performed in accordance with the DRDME-EA Purchase Description, dated 16 November 1977, and the MERADCOM Semiconductor Device, NPN Silicon Transcalent Transistor Specification, dated 25 April 1978, attachments Nos. 1 and 2, respectively, to the contract. The scope of the contract covers the MM&T projects for fabricating the semiconductor power device through an engineering phase, a confirmatory phase, and the subsequent pilot production of the device. The total number of devices to be fabricated in all three phases is 40 over a period of twenty-four months. Electrical, mechanical, thermal, and environmental inspections are a part of this contract effort as well as data and reports per DD 1423, Exhibit A of the contract.

This report, sequence No. A008 of the DD 1423, has been prepared in accordance with the referenced Data Item Description DI-S-1800 and Addendum thereto.

[1] S. W. Kessler, R. E. Reed, D. R. Trout, "Development of a High Voltage and High Current Transcalent Transistor" Final Technical Report, Nov. 1977, MERADCOM Contract No. DAAK02-72-C-0642.

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I. INTRODUCTION

This Final Technical Report describes the work performed by RCA, Lancaster, Pa., under the subject contract during the period 2 April 1979 through 30 March 1980. Work was initially performed in accordance with the DRDME-EA Purchase Description, dated 16 November 1977, and the MERADCOM Semiconductor Device, NPN Silicon Transcalent Transistor Specification, dated 25 April 1978, Attachments No. 1 and 2, respectively, to the contract. The scope of the contract was to cover the manufacturing methods and technology (MM&T) projects for fabricating a semiconductor device, silicon Transcalent Transistor, designated type J15381, and the subsequent pilot production of the device. At the completion of the engineering phase requirements as set forth in SLINS 0001 and 0004, RCA decided to phase out of the Transcalent solid state device business and therefore requested a modification to the contract. During the negotiations stages of this request, engineering work continued with the confirmatory devices in mind. Even with the reduction in scope signifigant progress in device refinement and operation was made.

A. Modification to the Contract

An unsolicited proposal, No. DP8165A was submitted 19 November 1979 as a modification to this contract. To this end a mutual agreement to complete the contract by the delivery of an additional five Transcalent transistors from residual inventory which meet the minimum engineering sample requirements and one sample with increased emitter area for a total of six additional units, Also included are the preparation of this document and the preparation of a separate summary report covering application notes and recommendations.

II. DESCRIPTION OF THE DEVICE

A. Transcalent Structure

Transcalent means permeable to heat flow, and best describes a new family of high power, solid state control and switching devices which have heat-pipes adjacent to each side of the silicon transistor wafer. An outline drawing of the Transcalent transistor is shown in Figure 1.

The Transcalent transistor, type J15381, is a triple diffused, bipolar NPN silicon transistor assembly mounted in a ruggedized, heat-pipe cooled military package with integral fins for forced air cooling. Both high voltage and high current capabilities have been achieved in small size, light weight assembly that has a large safe operating area (SOA).

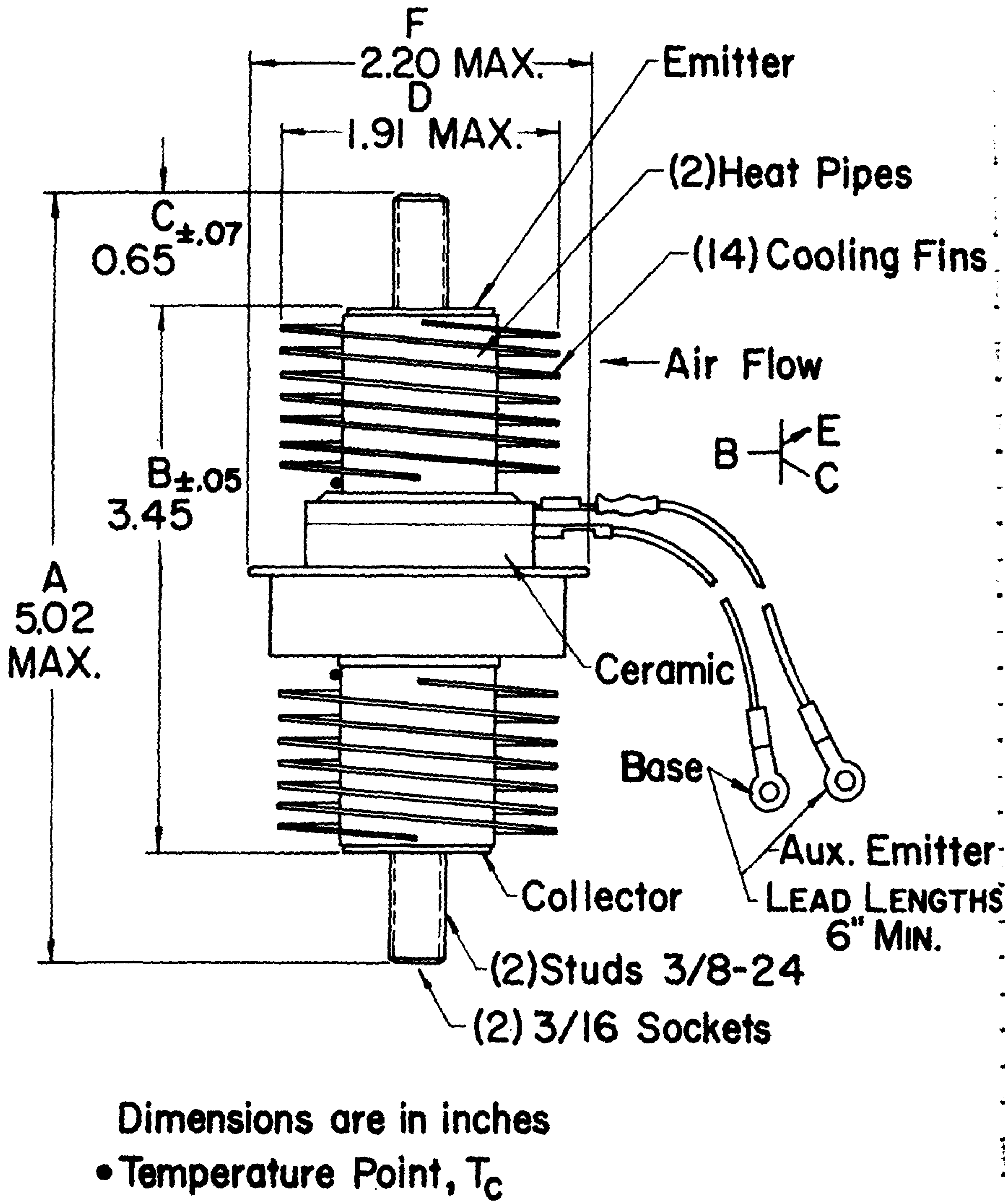

Figure 1 Transcalent NPN Transistor Type J15381 Outline Dwg.

The extremely small size (2" diameter, 3½" length - including heat sinks), light weight (12 oz.) and easily cooled (150 cfm of air) device belies the large ratings of 100 amperes, 750 volts and a dissipation rating up to 400 Watts. The heat-pipe endows the Transcalent transistor with an unusual thermal impedance characteristic which decreases with increasing amounts of power to be dissipated and at higher operating ambient temperatures. Internal emitter ballasting assures the proportionate sharing of current between the interdigitated emitter fingers.

The unique characteristics require fabrication techniques not normally found in the solid state component industry. These techniques include bonded heat sinks, chemically vapor deposited (CVD) tungsten metallized silicon chips, void-free soldering and vacuum processed assemblies. Those techniques combined with metallized ceramic insulators, heliarc welded assemblies and Boron swamping of possible conductive "pipes" in the silicon have all been utilized by RCA specifically for Transcalent power devices.

The heat-pipes attached to the silicon constitute a self-contained thermodynamic system which exhibits an effective thermal conductivity several orders of magnitude greater than copper[2]. This high thermal conductance is achieved by evaporation of a heat transfer liquid from the capillary or wick structure in thermal contact with the silicon, the transport of the vapor to other parts of the heat-pipe, condensation of the vapor along the walls of the pipe, and return of the condensate to the evaporator section through the capillary structure lining the inside wall of the heat-pipe. The two heat-pipes are joined together by the ceramic-to-metal insulator envelope which also provides a chamber for an inert gas atmosphere at the critical heat-transfer interfaces and around the passivated, contoured edge of the silicon chip.

The use of a wick structure distinguishes the heat-pipe from other reflux systems. Even with the heat-pipe orientation having gravity forces acting against the condensate returning to the evaporator, the wick furnishes sufficient capillary pumping force by the surface tension of the liquid to return the liquid to the evaporator for repeating the heat-transfer cycle. In addition, the capillary structure holds a thin film of heat-transfer fluid at the evaporator's hot surface.

[2] G. Y. Eastman, "The Heat-Pipe", Scientific American, Vol. 218, No. 5, May 1968, pp 38-46.

This thin film of liquid improves the heat transfer by preventing the formation of vapor bubbles close to the surface being cooled and thus improving the heat-transfer coefficient.

In the Transcalent power devices, water is the preferred working fluid because of the temperature range in which silicon transistor and other devices operate. Water has the greatest latent heat of vaporization, a large surface tension, and is compatible with the metals of the heat-pipe. The heat-pipes are essentially isothermal with equal amounts of heat being dissipated with equal efficiency by all of the fins This feature gives freedom in the geometric design of the heat-pipe and also means that an equal amount of heat can be transferred by all of the fins of the Transcalent device regardless of how far the fins are away from the silicon. Dimensions are limited only by the ability of the wick to "pump" the condensate back to the hot surface area where the liquid can be re-evaporated and the cycle repeated, the quantity of heat to be dissipated, the type of cooling (natural convection or forced air) to be utilized and the device weight permitted by the system design.

The transistor produced in this MM&T program is a three-terminal hybrid, heat-pipe cooled, silicon power switching transistor utilizing proven concepts in the Boron/Phosphorus diffused chips, CVD metallizing, edge contouring and a vacuum envelope that includes a high-strength, high alumina ceramic insulator designed to hold-off the required high voltages, even at reduced atmospheric pressure. The device is double-sided cooled with forced air directed at the integral fins of the heat-pipes. The heat-pipes provide superior cooling, even at high ambient air temperatures. The device is inherently rugged and reliable.

The Transcalent transistor type J15381, is designed to make maximum use of the integral heat-pipe thermal package, developed previously for the Transcalent rectifier[1].

A cross section of the device is shown in Figure 2 with a heat-pipe attached to each side of the active section. In operation, current is conducted to and from the silicon chip by the low inductance, high conductivity copper heat-pipes[2]. The studs at the ends of the heat-pipes are for fastening the high current leads to the device. The base and auxiliary emitter leads are for attachment of the control signal to the transistor.

[1]U.S. Patent 3,605,074, "Electrical Connector Assembly Having Cooling Capability" R. A. Freggens, and W. E. Harbaugh

[2]U.S. Patent 3,984,861, "Transcalent Semiconductor Device, etc.", S. W. Kessler

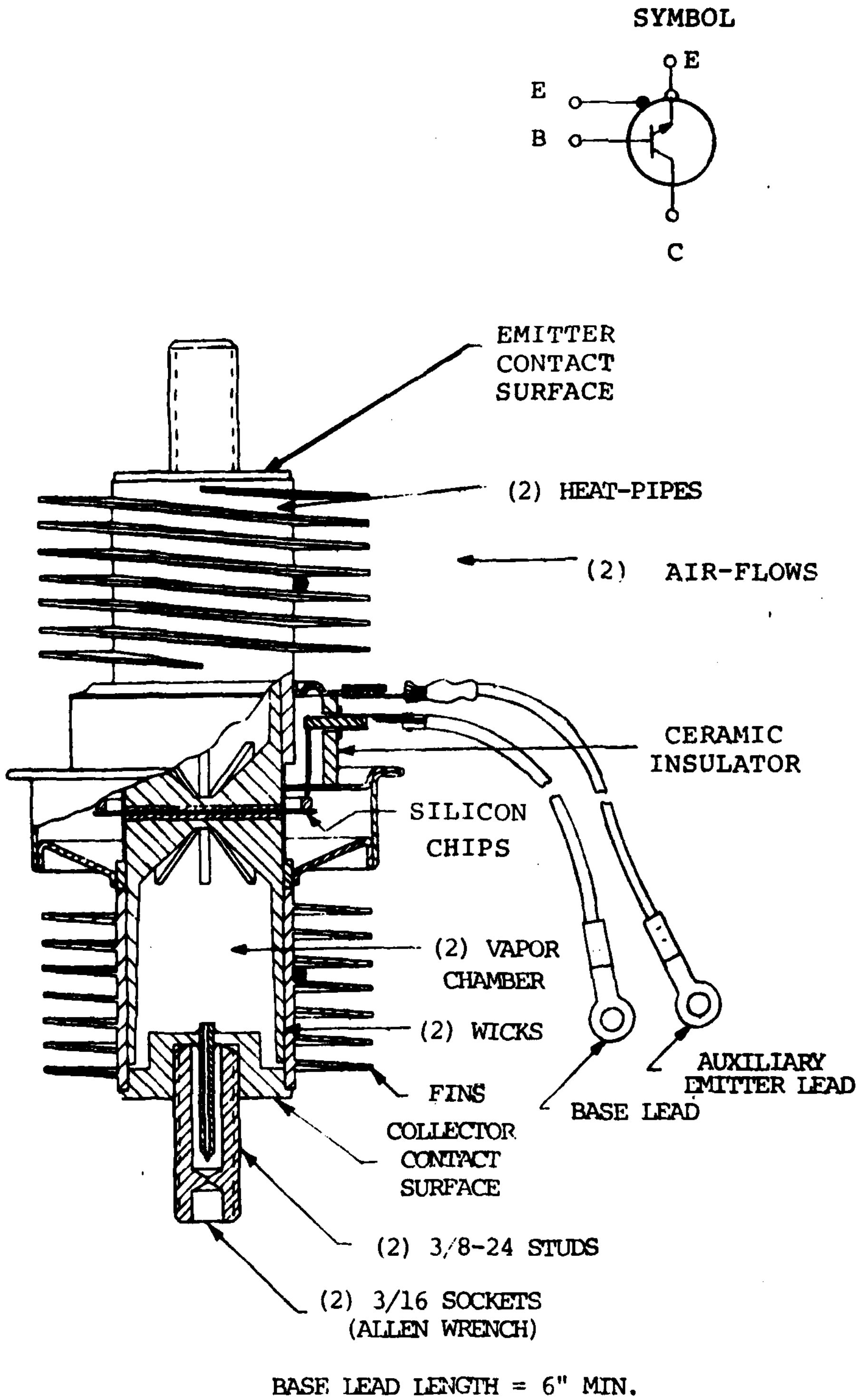

Figure 2 Transcalent NPN Transistor Type J15381 Cross-Section Drawing

A ceramic insulator and metal envelope are constructed between the two heat-pipes This envelope is the main structural member joining the two heat-pipes and minimizes any external stress transmitted to the weaker silicon chip. Heat which is generated in the silicon chip (an active transistor wafer and a passive emitter ballast wafer) during operation is conducted into the heat-pipes through the molybdenum discs closing the end of the heat-pipes adjacent to the silicon. The thickness of the molybdenum disc is optimized to have a minimum temperature rise in the silicon wafer during a single cycle of surge current by balancing the absorption and conduction of the heat[1]

Next, the heat is transferred into the porous copper wick adjacent to the molybdenum disc. The pores of the wick are filled with water which when evaporated, transfers heat to all parts of the heat-pipe by its latent heat vaporization. Since the heat-pipe is an evacuated vessel, evaporation occurs at all temperatures, (including below freezing by sublimation) and the vapor pressure can be interpolated from the vapor pressure curves for water. When vapor condenses at the coolest point in the heat-pipe, the vapor gives up its latent heat of vaporization. The condensation heat is conducted through the wall of the heat-pipe to the fins and dissipated to the air by the cooling fins. Since the vapor condenses at the coolest point, the heat-pipe is essentially isothermal with equal amounts of heat being dissipated with the same heat transfer coefficient by all of the fins. The condensate is returned to the evaporator by the capillary forces of the pores of the wick, as described above.

B. Advantages and Features

This double-sided heat-pipe cooled transistor is inherently rugged, as verified by the environmental tests performed during the engineering phase, and has unique advantages. Applications experience with Transcalent devices has demonstrated their superiority over conventional "hockey-puck" or "stud-mounted" devices, namely:

1. There are no external mechanical clamps fastening the device to the heat sink. Industrial experience indicates that the large clamping force relaxes through creep of cooper and aluminum during the life of the "hockey-puck" transistor. Inadequate cooling and lossy electrical contacts may thus result with the conventional devices.

[1] S. W. Kessler, "Development of a 250 Ampere Transcalent Rectifier", Final Technical Report June 1970 Contract No. DAAK02-69-C-0609.

"Hockey-puck" supplier's literature is full of cautions in mounting and torquing the bolts when clamping a device between heat sinks Over-torquing may crack the silicon. The heat sinks of a Transcalent transistor are an integral part of the device and require no clamps.

2. Heat is extracted from both sides of the silicon with a minimum of solid material adjacent to the silicon. This arrangement produces a low-temperature gradient between the junctions and the ultimate heat sink.

3 In operation the heat-pipes are very tolerant to changes in power level because of their ability to respond quickly by evaporating an additional amount of working fluid. They exhibit a decreasing thermal resistance as the power level increases.

4. Operation at higher ambient temperatures is possible without current derating.

5. Transcalent devices are of smaller size and lighter weight than hockey-puck devices with similar ratings, because of the greatly reduced temperature gradient between the junction and the fins. Also, all of the fins are equally effective in dissipating heat because the heat-pipe is isothermal along its entire length.

6. Corrosion resistant electro-plating and conformal coatings are utilized on the finished Transcalent transistor to enable it to withstand moisture, salt fog, and other hostile military environments.

7. Either end of the Transcalent transistor may be operated at ground potential, if required in the system design.

8. Transcalent devices conserve materials because much of the internal space of the device is hollow with a vacuum environment. Lighter weight results and a higher ratio of strength-to-weight is achieved.

III. PROCESS AND FABRICATION IMPROVEMENTS

Investigations are discussed in the following sections which had as their objective a reduction in the cost either by reducing the man hours required to perform the task or by improved yield and quality. That is, improved quality reduces the cost by providing a greater yield of acceptable product. Quality is particularly important in minimizing the cost of manufacturing a diffused and metallized wafer.

A. Processing of the Transistor Wafers

The Transcalent transistor employs a triple diffused structure. Two basic steps are employed to create the structure; they are: deposition of a dopant either with or without an oxide mask and the diffusion of the dopant to a desired depth to form a junction. The oxide mask is formed by thermally oxidizing the wafers, subsequently exposing a photo resist coating on top of the oxide to a mask pattern, and then by etching away the oxide in the open areas of the mask to permit the deposition of a dopant in these open regions.

Phosphorus is used for the n-type dopant and boron is used for the p-type dopant. All of the operations, such as cleaning of the wafers, and the control of surface concentrations center about the deposition and diffusion steps TABLE 2 outlines the sequence of operations in generating the triple diffused structure used in the Transcalent transistor. Only those operations which were considered excessively time consuming or which had poor quality with a yield that was low were investigated in the engineering phase of this contract.

The metallizing operations are performed after the diffusion operations as outlined in TABLE 3.

Process record cards travel with each lot of wafers through all of the operations. Blank copies of the record cards for the diffusion and metallizing operations are shown in Figures 3, 4, 5, and 6. If a number is assigned to each wafer, the number is scratched in the surface and near the edge of the wafer. On the back of each record card is a space for recording the characteristics measured for each wafer. Such data is useful in correlating process parameters with electrical characteristics. The operator also records his initials, date of the operation and the observed measurements Measurements other than the sheet resistance after etch back and the final electrical characteristics are made on control wafers which do not contribute to the final number of wafers in the lot.

Those operations which were investigated for possible improvement are discussed in the following paragraphs.

1. Neutron Transmutation Doped (NTD) Crystal

The method of doping the starting crystal was evaluated by processing two groups of wafers. The control group of wafers used phosphorus doped float zone crystal while the experimental lot of

TABLE 2

TRANSISTOR DIFFUSION OPERATION SEQUENCE

1. Clean the wafers.
2. Deposit phosphorus on both sides of the wafers using a $POCl_3$ source.
3. Chemically remove the phosphorus doped glass formed on the wafers during the deposition operation.
4. Clean the wafers.
5. Oxidize the wafers in steam.
6. Chemically remove the oxide from one side of the wafers.
7. Chemically remove the phosphorus doping from the side stripped of its oxide by etching away part of the wafer thickness.
8. Clean the wafers.
9. Deposit boron on the unoxidized side of the wafers using a boron nitride source.
10. Chemically remove the boron doped glass formed on the wafers during the deposition operation.
11. Clean the wafers.
12. Diffuse the boron and phosphorus dopants into the wafer to form the junction.
13. Etch off a small amount from the p-doped side of the wafers to secure the desired surface concentration.
14. Clean the wafers.
15. Oxidize the wafers in steam.
16. Apply photo resist to the p-doped side of the wafers.
17. Expose the resist to the emitter mask and remove the oxide from the emitter regions of the transistor using buffered acid.
18. Deposit phosphorus in the emitter areas of the transistor.
19. Chemically remove the phosphorus doped glass in the emitter regions.

TABLE 2 (Continued)

20. Clean the wafers.

21. Oxidize the wafers in steam.

22. Apply photo resist to the emitter side of the wafers and expose them to the p+ mask. Remove the oxide from the base regions of the transistor using buffered acid.

23. Clean the wafers.

24. Deposit boron in the p+ regions of the base using a boron nitride source.

25. Chemically remove the boron doped glass.

26. Clean the wafers.

27. Diffuse the emitters to achieve the desired peak gain.

28. Chemically strip all of the oxide from the wafers and clean the wafers.

29. Oxidize the wafers in steam.

30. Apply photo resist to the emitter side of the wafer and expose them to the moat mask. Remove the oxide from the moat regions of the wafer using buffered acid.

31. Etch a moat in the silicon to 1/2 to 2/3 the emitter junction depth.

32. Clean the wafers.

33. Oxidize the wafers in steam.

34. Etch the oxide in acid vapors for several minutes.

35. Chemically vapor deposit polycrystalline silicon on the emitter side of the wafers.

36. Densify the polycrystalline silicon.

TABLE 3

TRANSISTOR METALLIZING OPERATION SEQUENCE

1. Clean the wafers.

2. Apply photo resist to the emitter side of the wafers and open-up windows in the emitter and p+ regions of the transistor.

3. Chemically remove the polycrystalline silicon and oxide from the window areas.

4. Clean the wafers.

5. Evaporate palladium onto both sides of the wafers.

6. Chemically vapor deposit tungsten onto both sides of the wafers.

7. Electro-plate nickel onto both sides of the wafers.

8. Apply photoresist to the emitter side of the wafers and expose to the reverse tone of the mask used in operation No. 2. Use a continuous mask on the collector side of the wafer.

9. Remove the nickel, tungsten, palladium and polycrystalline silicon from open windows in the photoresist by etching.

10. Clean the wafers.

11. Electrically test the base to emitter junctions of each emitter finger.

12. Cut and contour the transistor chip from the wafer.

13. Etch and electrically test the base collector junction.

Transistor Diff. Process

Group No. ______ Wafer Lot No. ______ Bulk Res. ______ Wafer Th'k ______	# Wafers In	# Wafers Out	Date	Oper.
1. Clean				
2. Phos. Dep. 1100°C, 15/5/15 min.				
3. Pliskins Etch, V/I ______				
4. Clean				
5. Oxidation 1000°C, 6 hrs.				
6. Etch Oxide (Mask One Side)				
7. Etch Phos. Doping				
8. Clean (Optional)				
9. Boron Dep. 1150°C, 80 min.				
10. Glass Removal, V/I ______				
11. Clean				
12. Boron Diff. 1300°C ______ hrs. V/I ______ X_J ______				
13. Etch Back ______ V/I				
14. Clean				
15. Oxidation 1100°C, 4 hrs.				
16. Photoresist Emitter "A" Coat ______ Bake ______ Expose ______ Develop ______ Bake ______ Etch ______ Strip Resist ______				
17. Clean				
18. Phos. Dep. 1150°C, 15/20/30 min.				
19. Pliskins Etch, V/I ______				
20. Clean				
21. Oxidation 1100°C, 3 hrs.				
22. Photoresist Base "B" Coat ______ Bake ______ Expose ______ Develop ______ Bake ______ Etch (Mask One Side) ______ Strip Resist ______				
23. Clean				
24. Boron Dep. 1150°C, 80 min.				
25. Glass Removal				
26. Clean (Optional)				
27. Emitter Diff. 1250°C ______ hrs. Max. B ______ V_{ebo} ______ Base V/I ______				

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Figure 3 Transistor Diffusion Record Card (Front)

	# Wafers In	# Wafers Out	Date	Oper.
Collector V/I ______ X_{JN} ______ X_{JP} ______				
28. Clean				
29. Oxidation 1000°C, 135 min.				
30. Photoresist Moat "C" Coat ______ Bake ______ Expose ______ Develop ______ Bake ______ Etch (Mask Anode Side) ____ Strip Resist ______ Etch Moat ______				
31. Moat Etch Depth ______				
32. Clean				
33. Oxidation 1100°C, 60 min.				
34. 10% HF Vapor Etch				
35. Deposit Poly Si on Emitter Side				
36. Poly Si Densification/ Slow Cool				

Etch Back

Waf. #	V/I	Waf. #	V/I

Figure 4 Transistor Diffusion Record Card (Back)

Transistor Metallizing

Diffusion Group #____________________ Date __________

	Date	Oper.	# of Wafers In	# of Wafers Out
1. Oven Bake 200°C 1 Hr. Min.				
2. SC180, Expose				
3. (B) HF Etch 3 Min. R.				
4. FAN Etch______Sec.R.				
5. J100, J100, Hot Xylene Vap. Degr. Dry				
6. (B) HF Etch______Min. R.				
7. Caros Etch 5 Min. R.				
8. Wafer Wt._________mg.				
9. SC1, R, SC2, R.				
10. B(HF) 3 Min. R. & Dry				
11. Evap. Pd, Wt._________mg.				
12. CVD W, Wt._________mg.				
13. W Etch 15 Sec., R.				
14. Ni Strike, R & Plate, R & Dry				
15. Oven Bake 200°C 1 Hr. Min.				
16. SC180, Expose				
17. Wax Reverse Side				
18. Ni Etch, Rinse				
19. W Etch, Rinse				
20. 95/10-HNO_3/HF, 25s, R & Dry				
21. J100, J100, Hot Xylene Vap. Degr. Dry				
22. Meas. V_{EB}/Emitter				
23. Contour Wafer				
24. Wax Mask Both Sides				
25. Etch Ni & W				
26. Etch Junction 95/5-HNO_3/HF, 40 Sec. R & Dry				
27. Vap. Degr.				
28. Test, Record Data				

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Figure 5 Transistor Metallizing Record Card (Front)

Wafer No.	I_{CBO}		I_{EBO}		Max Beta	Comments	A Accept	R Reject	Wafer No.	I_{CBO}		I_{EBO}		Max Beta	Comments	A Accept	R Reject
	v	ma	v	ma						v	ma	v	ma				

Figure 6 Transistor Metallizing Record Card (Back)

wafers used neutron transmutation doped (NTD) crystal. The advantage of the NTD crystal is that there is only a small radial variation in the starting resistivity compared to as much as an 18 percent radial variation in the float zone crystal.

The control lot of wafers had a 75 percent yield of base collector junctions with 800 volts or greater, while the NTD lot of wafers had a 60 per cent yield. Also, the leakage current of the junctions diffused into the NTD crystal was an order of magnitude greater than the junctions diffused into the float zone crystal. However, since a small sample size was used, it would be premature to attribute the observed differences solely to the starting crystal. Differences greater than these have been observed between lots of wafers in which the process parameters were considered standard. With further investigation, it may be found that both float zone and NTD crystals can be used to fabricate Transcalent transistors.

2. Ion Implantation

Three small groups of wafers were ion implanted to investigate the possibility of eliminating the tight controls necessary to etch back a conventional diffused wafer to the desired surface concentration or surface resistivity (operation #13, TABLE 2).

The wafers employed had one side etched and an oxide grown on each. The intent was to implant the boron through the oxide and thus protect the wafers from contaminations which could form pipes in the diffused layer. Then any contaminants along with the thin oxide could be removed by etching prior to the diffusion operation (operation 12, TABLE 2). Pipes in the silicon are n-type channels in the boron diffused p-type layer. Pipes severely degrade the blocking voltage capability of the junction.

The three implanted levels of doping were 9×10^{13}, 1×10^{14} and 2×10^{14} atoms/cc. Of the seven wafers contoured and tested only one had an acceptable blocking voltage of 830 volts at a leakage current of 120 μA. This wafer had been doped to a level of 2×10^{14} atoms/cc and had a surface resistivity of 31.0 ohms. Most of the other wafers failed to block 200 volts and for this reason, ion implantation was not pursued further

It was further noted that the oxide film on the wafers made them more difficult to handle with the air belts on the ion implanter because a static charge gathered on the wafers which prevented movement.

3. Etch Back Experiments

The wafers are etched backed to the desired surface resistivity on the etching wheel shown in Figure 7 (operation 13, TABLE 2). The wafers are held in a PVC/Teflon fixture which masks the phosphorus doped collector side of the wafer to protect that side from etching. The etching solution is a mixture of hydroflouric, nitric and acetic acid which take many minutes to remove the desired amount of silicon.

In an effort to reduce the etching time, experiments were made using the basket etching station shown in Figure 8. At this station, a coin stack of 12 wafers was etched for one-fourth the time. The etching rate is enhanced by the heat of reaction from the 12 wafers versus one-half of a wafer per beaker when the wheel is used.

The reaction is quenched by removing the basket and wafers from the tank and inserting them into water. After a few minutes of basket etching, the wafers are in a wide range of low resistivity. This range is too wide to continue the etch at the basket etching station, so that the wafers are then grouped according to their resistivities and the etch is continued briefly on each wafer at the etching wheel station. The latter etching time varies according to the remaining amount of silicon to be removed. The actual total etching time using the two etching stations was reduced to nearly one-third that required when using the etching wheel alone.

This new process would have its greatest value when working with wafer lot sizes larger than the 23 wafer lot size employed in this contract.

None of the devices fabricated during this contract were produced using the combined etching stations. Further tests would be necessary before the process could be adopted. This is because etching occurs on both sides of the wafer and thus removes the damage lapped collector surface. A lapped surface is know to act as a getter during the diffusions. Gettering is the trapping of heavy elements in the dislocations near the surface of the silicon to prevent voltage degradation in the wafers.

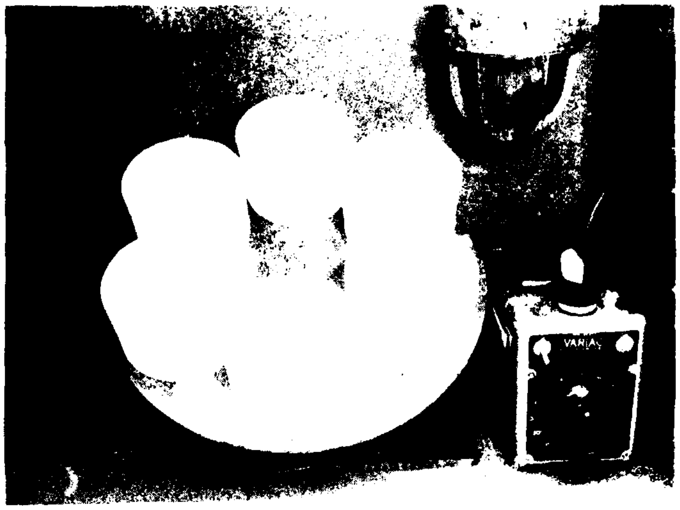


Figure 7 Etching Wheel and Fixtures

The speed at which the wheel rotates is controlled by the Variac. The wafers in the PVC/Teflon fixtures rotate within each beaker.

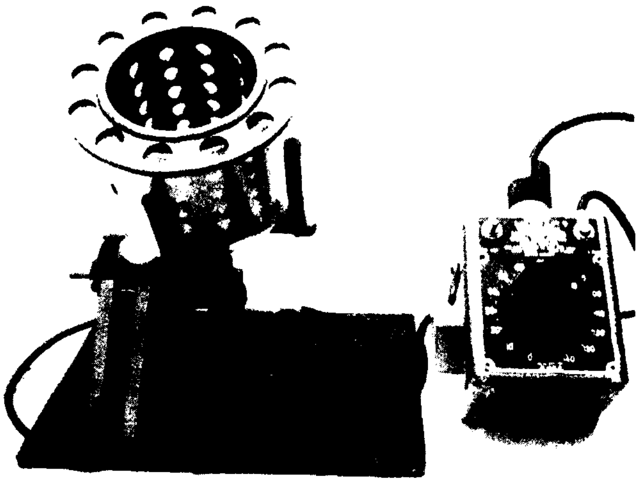


Figure 8 Basket Etching Station

The speed at which the basket rotates is controlled by the Variac.

4. New Photo-Masks

The following improvements were made in the mask design and were incorporated into the wafers diffused for the confirmatory phase of this contract.

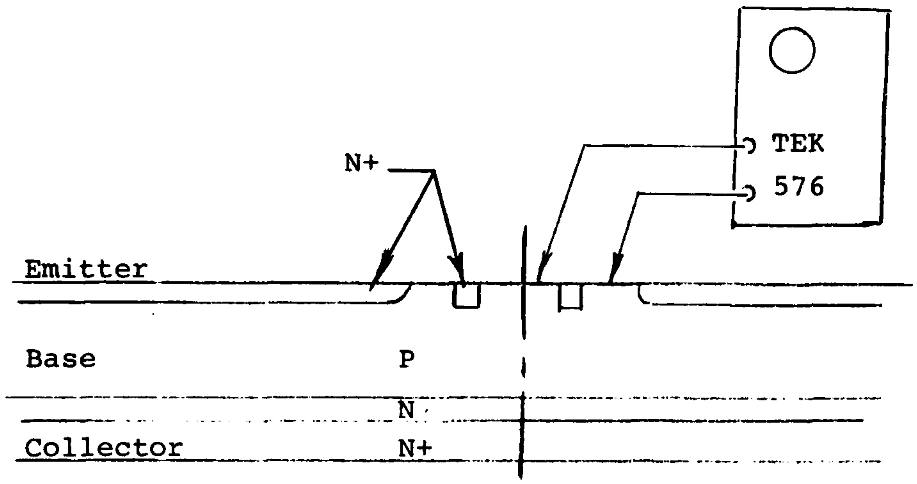
a. The diameter of the emitter patter was increased from 0.800 to 0.840 inch. This small increase in the diameter increased the total emitter area by 14.3 percent with a corresponding increase in the potential current conducting capability of the transistor.

b. A shunting current ring was incorporated in the center of the emitter pattern. A cross-section of the wafer in the region of the ring is shown in Figure 9 along with the circuit for measuring the current. The junction formed beneath the ring forces the current flow deeper into the silicon so that the measured current is indicative of the base resistivity. By knowing the base resistance of each wafer prior to emitter diffusion it is possible to select for each wafer an optimum diffusion time. With such a method of control, it would be possible to relax the tight tolerance on the surface resistance measurement at the etch back operation.

   Figure 10 shows the correlation of the shunting currents measured before and after two different diffusion times to the lot of wafers made for the confirmatory sample devices. The measurements were made at five volts. The gains, h_{FE} for the two diffusions were the peak gain measured on control wafers without metallizing. The moat etch and metallizing usually doubles the peak gain.

c. A method was incorporated for centering the mask pattern on the glass slide when the pattern is printed. This will reduce the accidental breakage of wafers at the mask aligner operation.

d. Two alignment marks at the outer edge of the mask patterns were changed from a doughnut shape to a tee shape. The tee shape is not only smaller but it has straight edges which make it easier to accurately position the wafer with respect to the mask. The new alignment masks thus reduce the time necessary to align each wafer at each of the photo resist operations.



Section A-A - cross section of the wafer in the region of the shunting ring showing the contact points for the Tektronix Type 576 curve tracer.

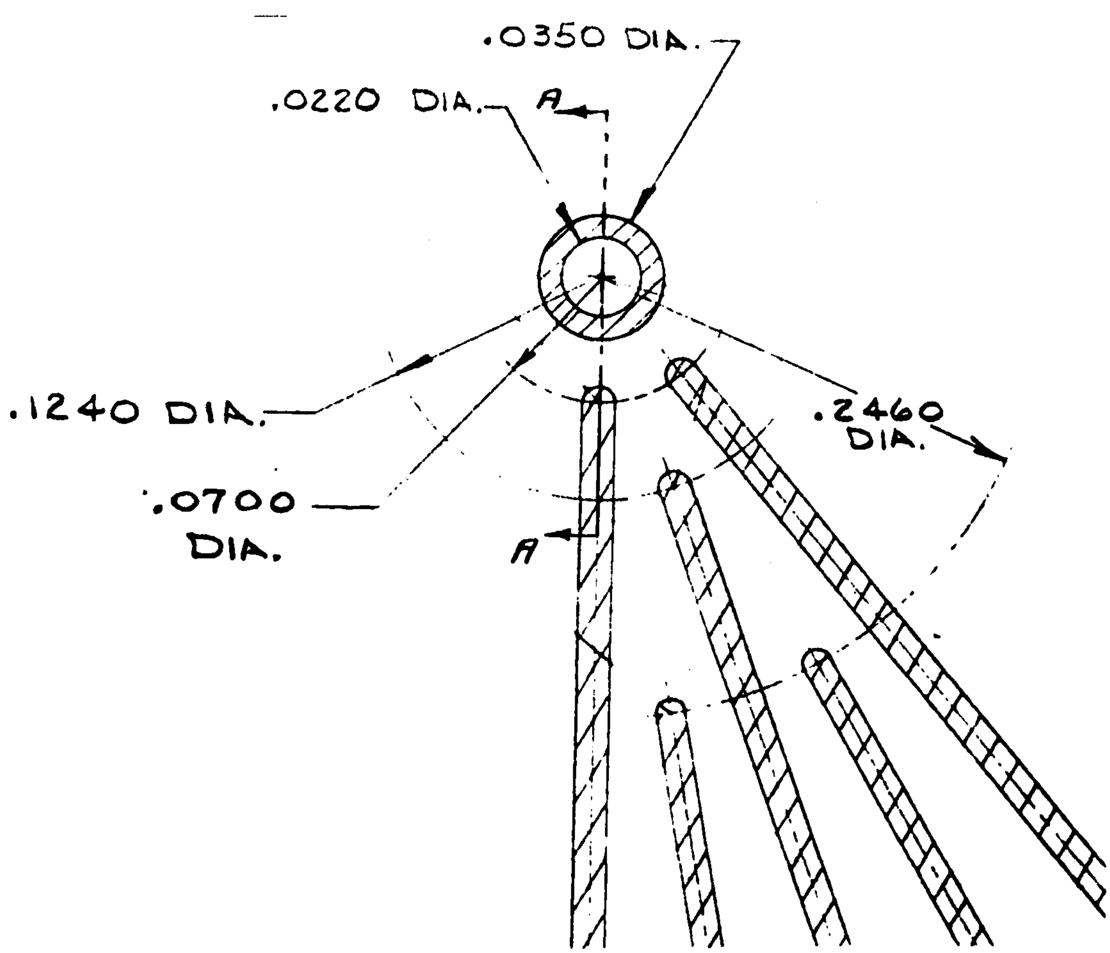


Figure 9

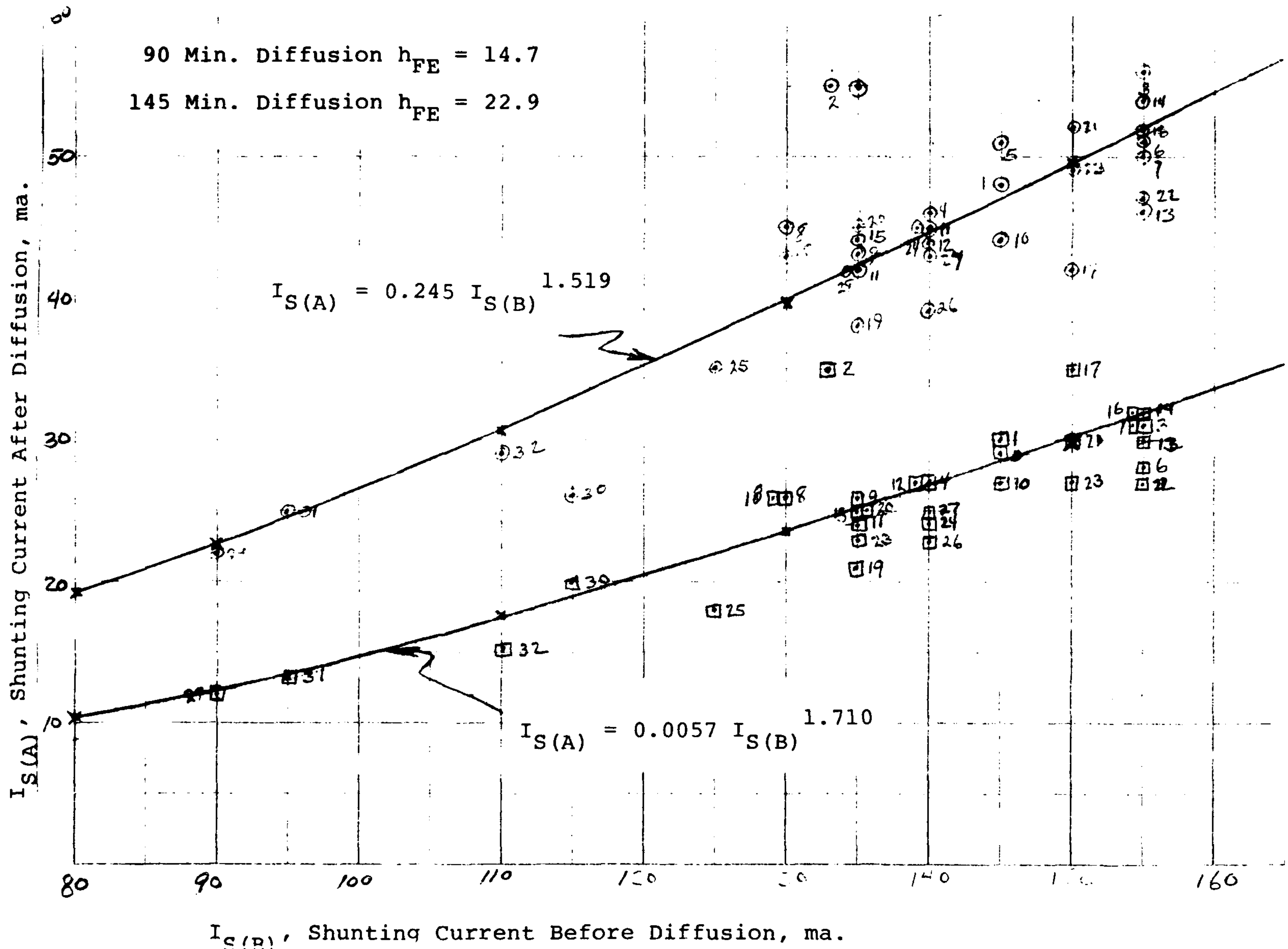

90 Min. Diffusion h_{FE} = 14.7
145 Min. Diffusion h_{FE} = 22.9
$I_{S(A)} = 0.245\ I_{S(B)}^{1.519}$
$I_{S(A)} = 0.0057\ I_{S(B)}^{1.710}$
$I_{S(A)}$, Shunting Current After Diffusion, ma.
$I_{S(B)}$, Shunting Current Before Diffusion, ma.

Figure 10

The new masks were received after the fabrication of the engineering samples because of the long lead time necessary to acquire photomasks. Chrome and iron oxide masks were made from the masters to provide working masks for wafer fabrication.

5. Cratering

When tungsten is chemically vapor deposited (CVD) on the wafers, there is a reaction between the acid vapor generated from the reduction of the source gas with hydrogen and the edge of the oxide passivating the base to emitter junction of the wafer. The product of the reaction is a strong etchant which can locally etch the silicon, creating a microscopic sized crater in the surface of the wafer. Since craters are known to affect the yield of acceptable base to emitter junctions, the following experiments were conducted to eliminate cratering or to minimize its depth.

Tungsten was CVD'd onto dummy silicon wafers at four temperatures. Each wafer was cross sectioned to observe the depth of the crater. The experimental wafers had the same oxide and polysilicon pattern on them as would be on a transistor wafer. At the next to hottest temperature the craters were 0.85 micron deep which is much shallower than that observed at the hottest normal deposition temperature. However, the deposition rate was only about 0.4 of that at the hottest temperature. At the two lowest temperatures, the deposition rate was too slow to be practical. It is thus concluded that a lower CVD temperature will reduce the depth of the craters but with an acceptable deposition rate.

In an effort to eliminate cratering, a group of device wafers was passivated with silicon nitride, Si_3N_4. A cross section of one of these wafers showed no signs of cratering after CVD tungsten at the normal temperature. A couple of devices have been fabricated since the engineering phase using the Si_3N_4 wafers. The only problem noted using Si_3N_4 were its inertness to etchants and that the facilities for its deposition are available only at other RCA plant locations.

6. Etching the Metallizing Pattern

A photo resist pattern is used to protect the metals on the base and emitter areas while the unwanted metal between these regions is etched away. This is the method used to define the metallizing pattern for the transistor wafers. The three metals; nickel, tungsten and palladium; which constitute the metallizing are etched in turn using one solution to etch the nickel, a second solution to etch the tungsten, and a third solution to etch the palladium and polycrystalline silicon on which the palladium is deposited. At the completion of the metal etching operation, the metals on the emitters are isolated from those on the base and each emitter is surrounded by the oxide passivating the base to emitter junction.

For this operation to be a success, the thin film of photo resist must be very adherent while being exposed to all three of these harsh etchants. Sometimes, even when the adherence is good, there is etching of the metal at the edge and slightly beneath the photo resist mask. This edge etching makes the width of the base and the emitter metallized areas narrower than desired.

To avoid edge etching, electrolytic etching of the nickel and tungsten was explored. It was found that the same etching solutions at one tenth of their normal strengths could be used for electrolytic etching of the pattern. Electrolytic etching is also much faster than chemical etching and by monitoring the current, it is possible to accurately observe the approach of the end point. At the end point, the etching current is nearly zero because there is no longer any anode area (wafer) in direct line of sight from the cathode. The desired metal pattern is insulated and protected by the photo resist. The edge definition obtainable with electrolytic etching is also better than with chemical etching.

The main disadvantage of electrolytic etching was observed when device wafers were etched. There was a large percentage of base to emitter shorts on the wafers. The shorts were so small that the etching current which the shorts conducted could not be differentiated from the small electrolytic current flowing at the end point of the etch. Futher investigation will be needed.

7. Base Metallization

The electrical conductivity of the base metallization is very important because it determines the length of each of the 72 emitter fingers that can be made active by the injection of current from the base. The base current is conducted to the emitters by the thin metallization layer on the silicon chip. Refer to Figure 11. A radial ohmic drop of about 26 mV will reduce the injected emitter current by a factor of 1/e or 37 percent.

To investigate this possible limitation, two transistors were made in which a layer of copper was substituted for the nickel plating which is normally deposited on top of the CVD tungsten layer. The copper layer reduced the base metallization sheet resistance by a factor of 5. A thin layer of gold was subsequently plated on top of the copper to aid in defining the metallization pattern. The test results are summarized in TABLE 4 along with another transistor made from the same lot of wafers which had the standard base metallization.

The results show that there was no increase in the current capability for the transistor with the copper metallization. The differences noted are within the normal distribution of the current capability for the Transcalent transistor.

B. Ballast Resistor Alternate Material

Each Transcalent transistor has a ballast resistor between the emitter surface of the transistor chip and adjoining surface of the emitter heat-pipe. The ballast resistor distributes emitter current to the 72 emitters. If the resistor has a positive coefficient of electrical resistance, the ballast resistor will also force proportionate current sharing between the emitters. This latter function is very important because it compensates for the negative change in the voltage drop across the base to emitter junction, V_{BE}, with increasing temperature.[1]

It is this negative change in V_{BE} which causes one region of an emitter to have a lower resistance with a corresponding increase in the localized emitter current which may take the transistor into a destructive thermal runaway mode of operation. The ballast resistor in the

[1]Semiconductor Power Devices, S. K. Ghandhi, Page 157, Para. 4.3.2. John Wiley & Sons

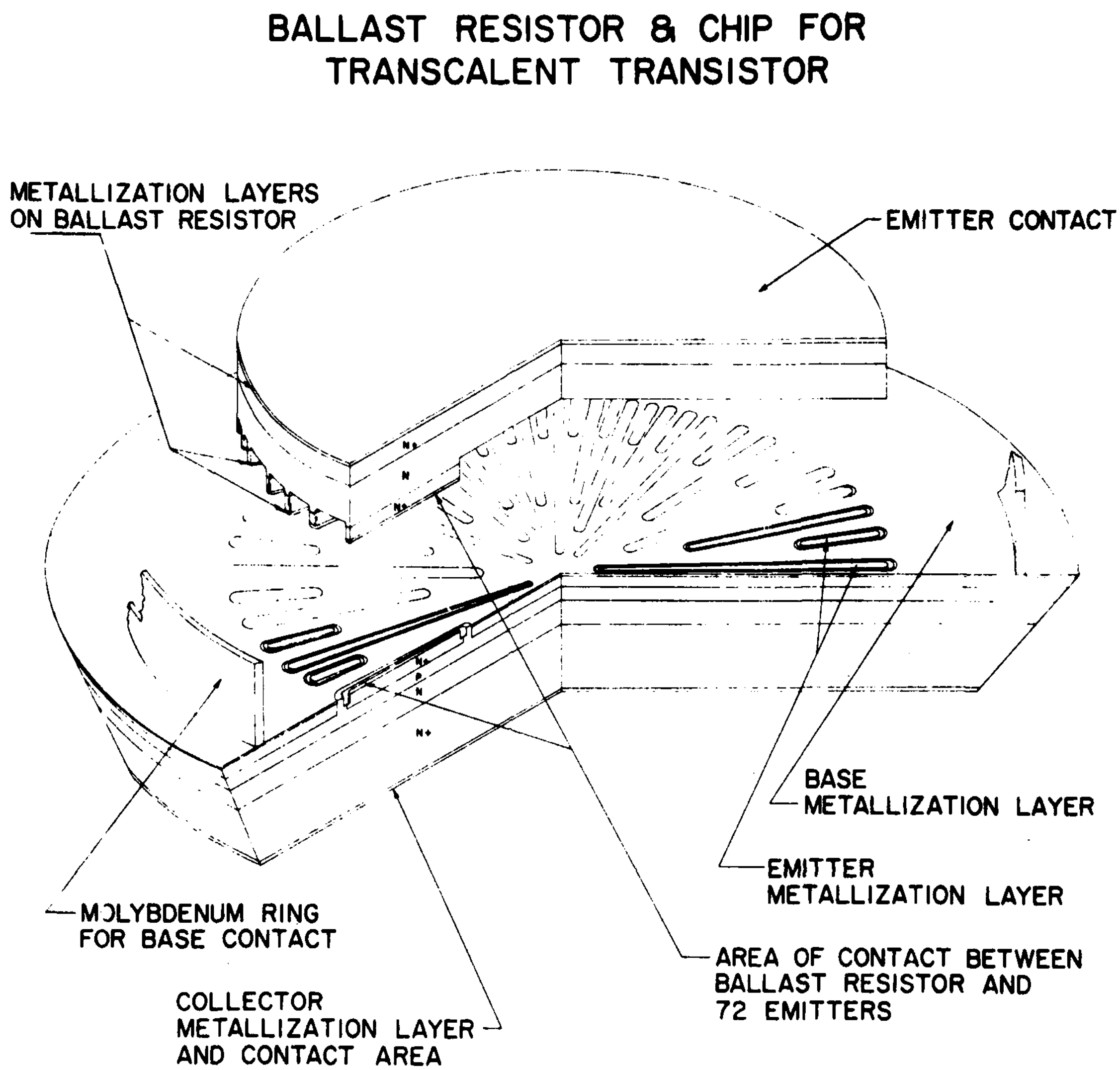


Figure 11 Complete Single Transistor Wafer Subassembly

TABLE 4

COMPARISON OF BASE METALLIZATION SYSTEMS

Metallization	Pd/W/Ni*	Pd/W/Cu/Au**	
Device No.	171	172	173
I_C @ V_{CE} = 1 V, I_B = 20 A	110 A	98 A	104 A
I_C @ V_{CE} = 5 V, I_B = 20 A	148 A	135 A	142 A

*Palladium/Tungsten/Nickel Metallization System.

**Palladium/Tungsten/Copper/Gold Metallization System.

Transcalent transistor was designed to protect the transistor from thermal runaway and this innovation has enabled the transistor to be operated at the very high currents mentioned in this report.

All of the ballast resistors used during the previous R & D contract (DAAK02-72-C-0642) and all but one of the engineering samples in this contract were made using heavily doped, low resistivity silicon (0.04 to 0.06 ohm-cm, n type). The procedure for fabricating these silicon ballast resistors is listed in Table 5. The desirability of simplifying this process is evident from the table. Many of the listed operations could be eliminated if the ballast resistors were made from a suitable metal disc.

For this reason tungsten was investigated as a potential alternate material to fabricate the ballast resistor. Tungsten's thermal expansion nearly matches that of the silicon; its thermal conductivity is about one third that of copper but better than silicon and its coefficient of electrical resistance is positive (similar to that of the specially doped silicon) at 2.47×10^{-2} ohm per degree Celcius. The simplified process used to fabricate the tungsten ballast resistor is listed in Table 6.

The processing may be further simplified by combining the etching of the mesas and the cutting into one operation. To do this, photoresist will be applied to both sides of the blank. One side will be exposed to the emitter pattern and the opposite side will be exposed to a ring nearly the same diameter as the emitter pattern. The masks for the two patterns will be prealigned in an exposure fixture.

When the tungsten is etched from both sides, the plane of etching at the extremes of the ring will join the plane surrounding the mesas, causing the resistor to be etched from the blank. The region of the ring over the ends of the mesas and on the opposite side of the disc will be etched to half the thickness of the tungsten, so that the ends of the mesa contacts will extend slightly beyond the inside diameter of the ring for use in the alignment step.

The ring mask will also have two etched alignment dots which will be located on each side of one of the longest emitter fingers on the emitter mask. The dots will be etched along with the ring thus identifying the rotational location from the plane side of the ballast resistor. The identifying marks will replace the pencil marks used at present in the final assembly operation (as described in Section III D3 of this report).

TABLE 5

SILICON BALLAST RESISTOR FABRICATION PROCEDURE

1. Dope both sides of the wafer with phosphorus to form ohmic surfaces,

2. Grow a thermal oxide on the wafers,

3. Apply a photoresist pattern and etch one side of the silicon wafer to form mesas having the same geometry as the emitters on the transistor.

4. Metallize both sides of the wafers using palladium, tungsten and nickel.

5. Apply a photoresist pattern and etch off the metals between the mesas. A continuous mask is applied to the opposite side of the wafer.

6. Apply a photo pattern and pulse plate a gold contact on top of each mesa. The gold is a soft metal which makes a low electrical resistance contact between the ballast resistor and the emitters of the transistor.

7. Cut the ballast resistor out of the silicon wafer. This operation is done with a precision sand blast nozzle with the sand directed at an angle such that a tapered edge is made around the periphery of the wafer. When the cut is completed, the ends of the mesas project slightly beyond the circumference of the solid part of the wafer. These projections are used, as is explained in the assembly section of this report, to align the ballast resistor with the transistor chip.

TABLE 6

TUNGSTEN BALLAST RESISTOR FABRICATION PROCEDURE

1. Nickel plate and fire the blanks in hydrogen.
2. Gold plate the blanks.
3. Apply a photoresist pattern. Etch both the gold and the tungsten to form the mesa contacts.
4. Cut the ballast resistor from the blank as was described in the process for a silicon wafer (Refer to TABLE 5).

Table 7 compares the measured emitter resistance of the experimental transistor, Serial No. J164, made with a tungsten ballast resistor to two standard transistors, Serial Nos. J162 and J163, each of which was assembled with a silicon ballast resistor. The measurements were taken at two different junction temperatures. Data from a previously fabricated transistor, J152, also using a tungsten ballast resistor is also included in the table for comparison. The J152 transistor was fabricated previously with RCA net engineering funds.

It was thus concluded that tungsten is at least equivalent to silicon as a ballast material for the Transcalent transistors and may be superior because of its consistent positive temperature coefficient.

C. Assembly of the Heat-Pipe

The procedures for assembling the heat-pipes for the Transcalent transistor are the same as those developed for the Transcalent thyristor, as were completely described in the Final Technical Report on MERADCOM/ECOM Contract No. DAAB07-76-C-8120, covering the period 27 September 1976 to 30 October 1978. In fact, the same brazing fixtures are used in making the heat-pipe subassemblies for the Transcalent thyristors, rectifiers and transistors. The only differences in the design of the transistor and the thyristor or rectifier heat-pipes are, as follows:

1. The molybdenum disc brazed in the end of each transistor heat-pipe is 0.050 inch thick versus 0.030 inch for the thyristor and rectifier.

2. A 0.032 inch diameter nickel plated copper wire is used for the internal base lead of the transistor versus a 0.015 inch diameter nickel wire used for the gate lead of the thyristor.

The thicker discs are employed in the transistor to minimize their deflection when the transistor is clamped together for welding. The larger base lead is used to reduce the electrical resistance of the internal base circuit for base currents of up to 10 amperes.

Figures 12 and 13 show cross sections of two devices. The cross section in Fig. 12 represents the device manufactured during the engineering phase and the package is similar to that of the Transcalent Thyristor manufactured under Contract No. DAAB07-76-C-8120. The drawing in Figure 13 shows the refinements engineered during this contract.

TABLE 7

COMPARISON OF BALLAST RESISTOR MATERIALS

Device Ser. No.	Ballast Material	Junction Temperature (^{o}C)	Re´ Emitter Resistance (Milliohms)
J152	Tungsten	32	3.23
		105	6.30
J162	Silicon	32	5.56
		105	6.45
J163	Silicon	32	4.65
		105	4.41
J164	Tungsten	32	4.44
		105	4.76

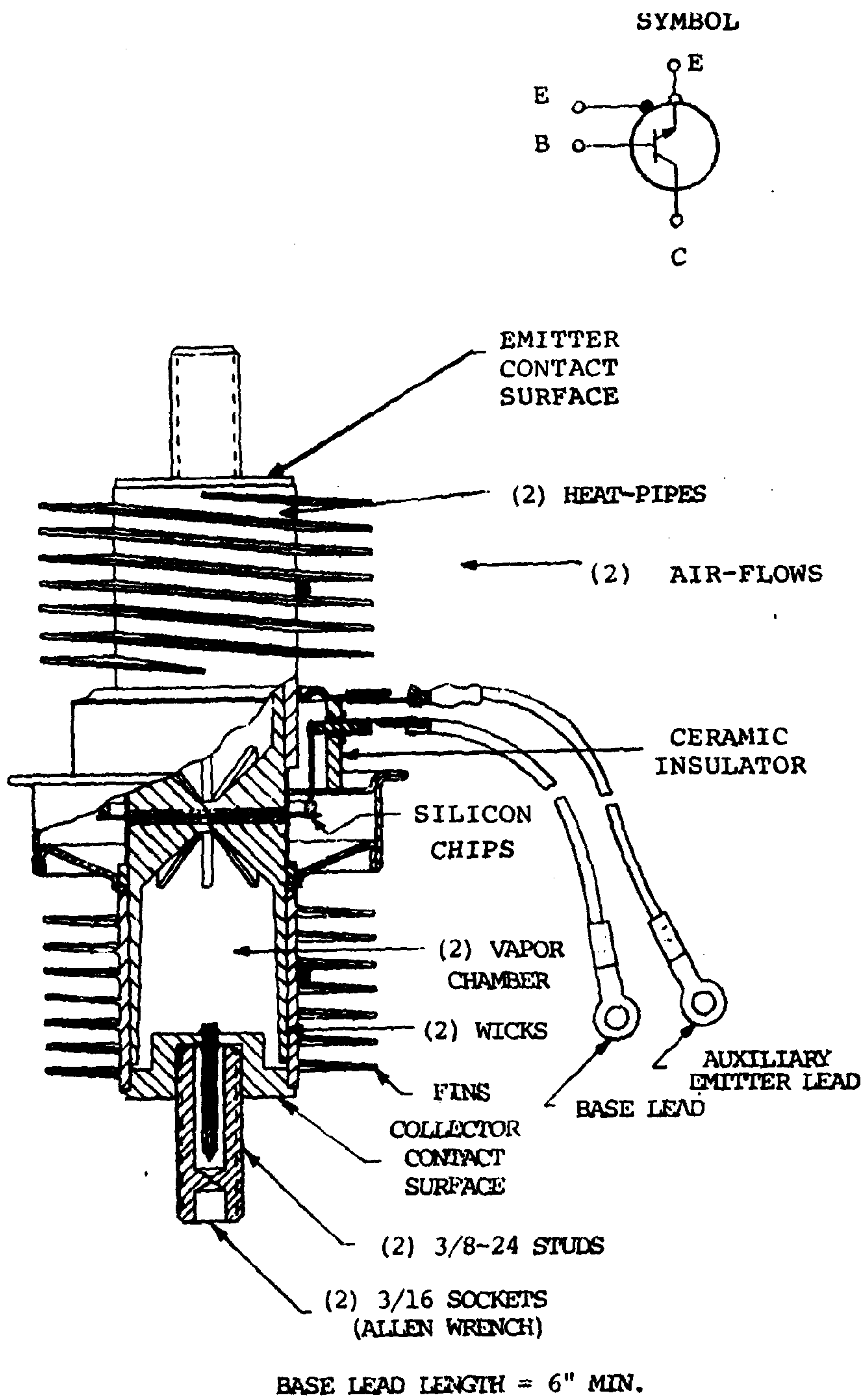


Figure 12 Initial Transistor Package Design Cross Section

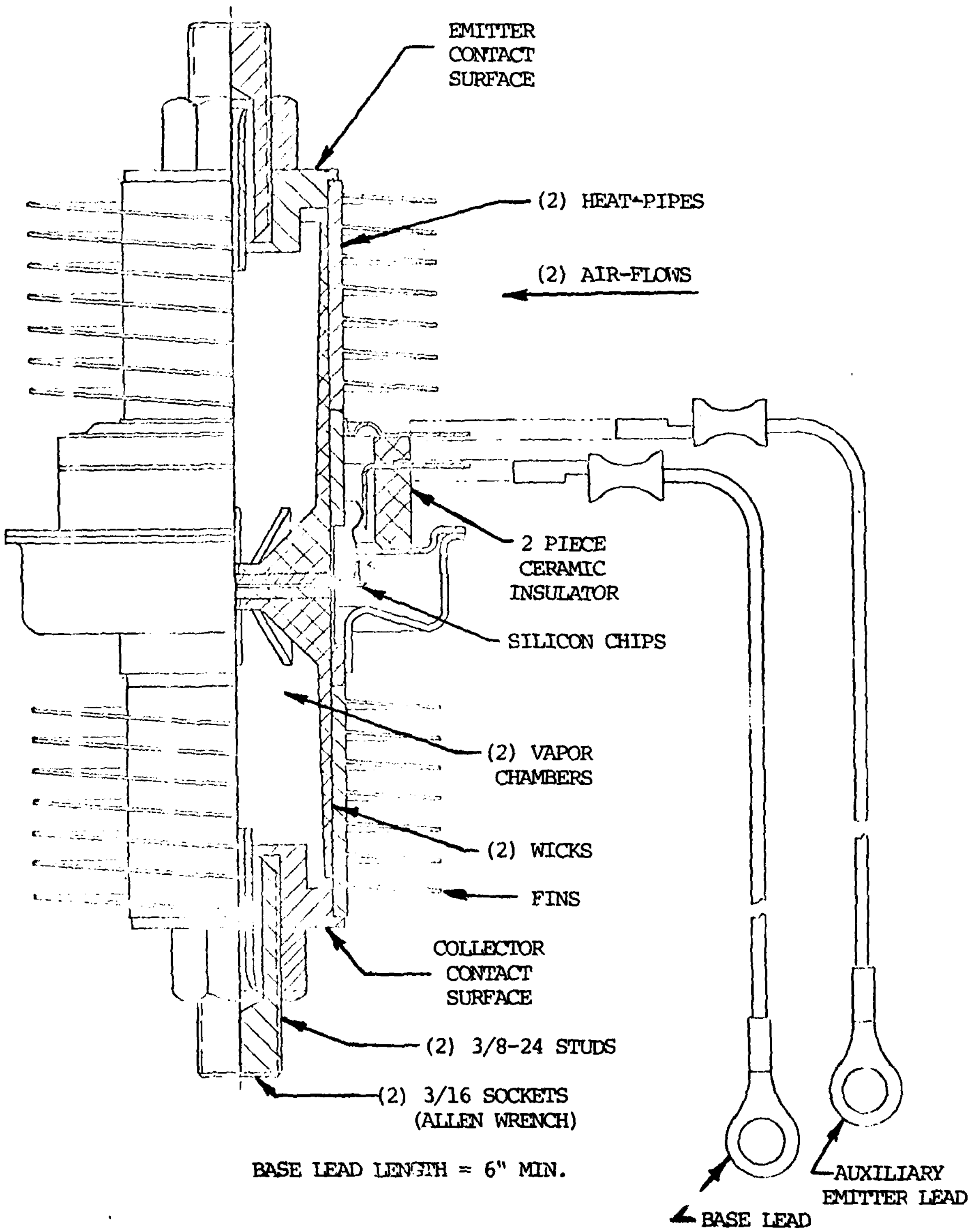


Figure 13 Refined Transistor Package Design Cross Section

The cross section in Figure 13 also shows a low inductance base contact ring soldered to the transistor chip. This ring is soldered to the chip during the final assembly operations and aids in distributing the base current to all areas of the transistor.

The cross section shown in Figure 13 illustrates several cost reduction features and design improvements which will be incorporated in the confirmatory samples. The most notable feature is the base connection which has substantially lower electrical impedance than that shown in Figure 12. This base configuration will be especially beneficial for future higher current variants of the transistor where base currents of 20 or more amperes are used.

The base connection shown in Figure 13 consists of a Kovar base feed-through ring and a circular, low inductance beryllium copper spring contact which is substituted for the original base connection design consisting of the Kovar pin feed-through and the nickel plated copper wire as shown in Figure 12. The feed-through ring is brazed between the two ceramic insulators. Along the outer edge of the base ring there are two quick disconnect tabs for attaching the external base lead. The berryllium copper spring is soldered to the transistor chip during the final assembly and makes mechanical contact to internal surface of the base ring when the heat-pipes are assembled. This new internal base lead design has much less electrical resistance and inductance than the single wire lead construction shown in Figure 12.

It should also be noted that the wall thickness of the ceramic insulators is greater in the new design. A thick wall ceramic is less costly to produce because it is more easily formed and less likely to warp in firing. Unnecessarily tight tolerances were also removed from the ceramic parts drawings in their redesign.

Also shown in Figure 13 is a redesign of the anode flange to eliminate one of the two closure welds. The separate anode flange and weld ring shown in Figure 12 were combined into one piece.

In fabricating the heat-pipes the evaporator end of each heat-pipe is lapped flat to insure better contact between the heat-pipe and the metallized silicon chip during final assembly. A new lapping machine was procured by RCA for this program to automatically lap 14 heat-pipe subassemblies simultaneously. This machine is shown in Figure 14.

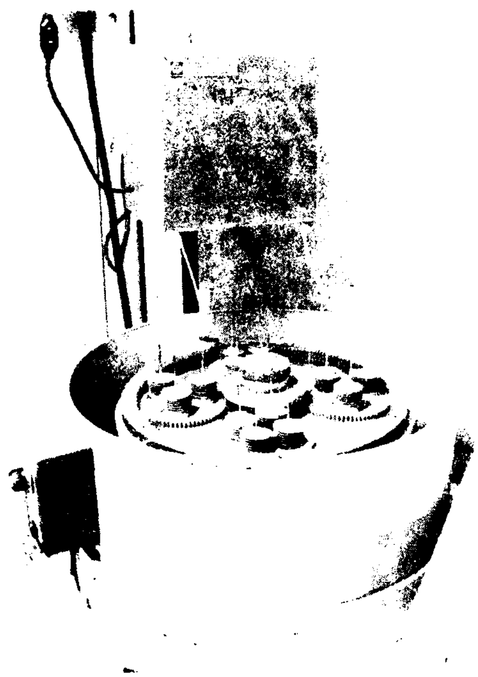


Figure 14 Automatic Lapping Machine which insures that the end of each heat-pipe (which contacts the silicon) is flat

D. Final Assembly of a Transcalent Transistor

The Transcalent transistor is assembled in the sequence listed in Table 8 as follows. Each of the operations in the table will be discussed in the following paragraphs with respect to the methods employed in fabricating the experimental devices on Contract No. DAAK02-72-C-0642, the fabrication of the engineering samples for this contract, and the proposed method of fabricating later devices.

1. Soldering of the Chip to the Heat-Pipe

a. Pretesting the transistor chip: Each transistor chip is considered suitable for soldering only after both sets of its junctions are electrically tested OK. The emitter base junctions formed between each of the 72 emitters and the base electrode are tested for V_{EBO} before the transistor chip is cut from the wafer and contoured around the outer edge.

The test is performed using the microprobe fixture shown in Figure 15. This fixture consists of 36 probes, each 10 degrees apart, which can be positioned to contact every other emitter on the wafer. By rotating the wafer 5 degrees, contact can then be made to the second set of 36 emitters. Connection is made to each of the emitters through a needle-pointed microporbe and a rotating selector switch. The electrical characteristics of each emitter to base junction is thus displayed, in turn, on a transistor curve tracer.

If the total leakage current of the 72 emitters is less than 50 mA at 8 volts, the wafer is acceptable for cutting and contouring. If the leakage is greater than 50 mA, the wafer is reprocessed through the photo resist and metal etching operations in an attempt to improve this leakage current.

The breakdown voltage of the base-to-collector junction, V_{CBO}, is measured after cutting and etching the positively contoured edge of the transistor chip. This measurement is made with a Tektronix type 576 transistor curve tracer. If the leakage current of this junction is less than 500 microamperes at the 750 volts, the transistor chip is considered suitable for soldering to the collector heat-pipe.

TABLE 8

FINAL ASSEMBLY SEQUENCE FOR THE TRANSCALENT TRANSISTOR

1. Solder a pretested transistor chip to the collector/anode heat pipe. At the same time the base contact ring is soldered to the chip.

2. Passivate the contoured edge of the silicon chip.

3. Assemble a ballast resistor to the silicon chip.

4. Clamp the emitter heat-pipe to the collector heat-pipe subassembly.

5. Solder the base feed-through wire onto the base contact ring.

6. Heliarc weld the weld ring to the flanges attached to both the emitter and collector heat-pipes.

7. Exhaust and back-fill each of the three chambers of the device. The two heat-pipes are back-filled with ultra-pure water. The chip chamber is back-filled with dry nitrogen.

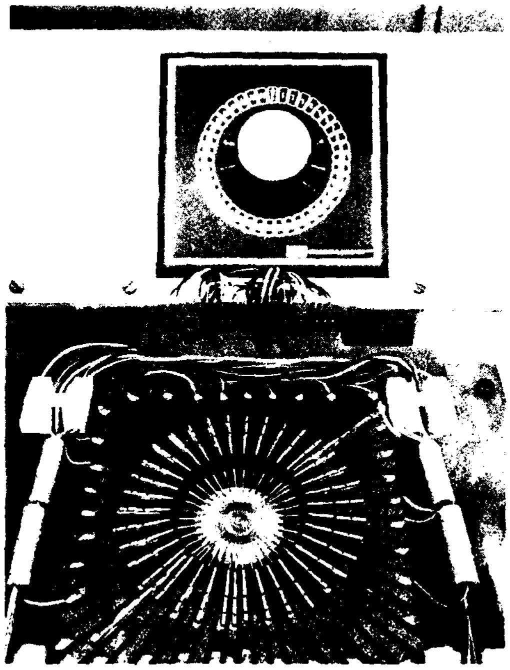


Figure 15 Microprobe Test Station for testing the V_{EBO} of each of the 72 emitters. The probe is connected to a curve tracer (not shown in the figure). Through the selector switch at the top of the photograph, 36 emitters can be tested in turn. By rotating the wafer 5 degrees the other 36 emitters can be tested. The V_{EBO} measurements are usually made before contouring the transistor chip.

b. Soldering

The transistor chip is soldered to the collector heat-pipe using a solder preform of lead-tin alloy. A photograph of the soldering fixtures is shown in Figure 16. The soldering procedure is proprietary to RCA. The procedure used produces a void-free interface having a lower thermal impedance than a mechanical interface. The soldered interface is also resistant to thermal fatigue.

2. Passivation of the Chip

The contoured edge of the transistor chip is passivated with a silicone resin after retesting for V_{CBO}. The resin is cured in an air oven at a moderate temperature.

As an alternate to the silicon resin passivation, silicon nitride (SI_3N_4) was investigated. If this technique were feasible a polysilicone deposition process could be eliminated from the fabrication of the transistor wafer. Also, there are no chemical reactions between the passivation and the hydrogen fluoride (HF) generated in the tungsten CVD system as there is when oxide passivation is employed.

Several wafers were fabricated using silicon nitride passivation at the periphery of the emitter-base junction. The following chemical reactions are involved:

$$WF_6 + 3H_2 \rightarrow W + 6\ HF \qquad (1)$$

where: WF_6 is tungsten hexafluoride gas,
H_2 is hydrogen gas, and
HF is hydrogen fluoride (hydrofluoric acid) gas.

$$2\ S_iO_2 + 6\ HF \rightarrow S_{i2}O\ F_6 + 3H_2O \qquad (2)$$

where: S_iO_2 is the silicon dioxide on the water,
$S_{i2}OF_6$ is silicon oxyfluoride, and
H_2O is water vapor

Two wafers were cross sectioned to examine the silicon for possible cratering or corrosive attack by the products of the metallizing process.

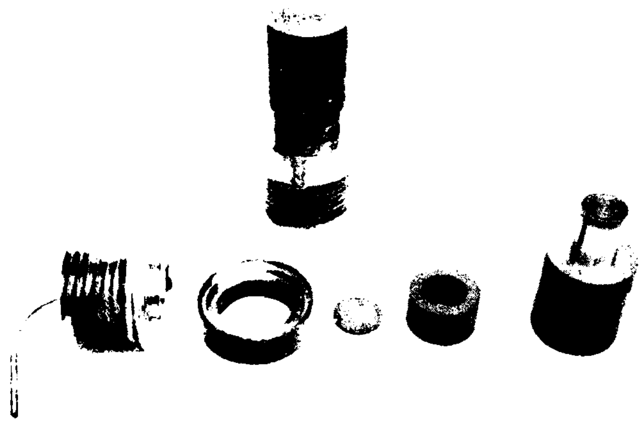


Figure 16 Transistor Soldering Fixture: The transistor chip is positioned with respect to the anode weld flange with the large ring near the center of the photograph. The disc next to the ring prevents solder from splashing onto the emitter area of the chip. The smaller ring weights and positions the base contact ring. The overall solder weight is the large part to the far right. At the top of the photograph is a complete fixtured assembly ready for soldering in a furnace.

The first wafer which was cross sectioned was done after the metallization pattern was delineated by photo etching. The results were confusing because the HNO_3/HF acids (nitric and hydrofluoric, respectively) which were used to etch the Palladium (Pd) also attached the silicon at the edge of the Si_3N_4 where cratering would normally be observed. The etched region was about the same depth as a crater would be but the surface was smooth compared to the typical ragged edges of a crater.

The second wafer was cross sectioned immediately after the W-CVD (chemical vapor deposition) plating. This wafer did not show any signs of etching or cratering, even at a microscope magnification as great as 1500X.

The conclusions drawn from these intermediate results are, as follows:

a. That Si_3N_4 passivation eliminates the potential formation of craters in the surface of the wafer. Craters are undesirable because they have the potential of growing into cracks in the brittle silicon. These cracks would subsequently degrade the electrical characteristics of the transistor. However, as long as the craters are shallower than the diffusion depth of the emitter junction, the electrical properties of the transistor are apparently not affected.

b. That an acid not containing HF should be used to etch the Palladium (Pd). HNO_3/HF had been used previously because standard wafers used a polysilicone covering over the SiO_2 passivation. Polysilicone is not used with Si_3N_4. The polysilicone was thus removed or etched at the same time as the Pd.

Finally, the base-to-emitter junction of ten of the wafers from this lot were passivated with silicon nitride. Although the metallizations of these wafers were excellent, the peak gain of the transistors failed to meet the specified minimum current gain of 20 times. One of the remaining wafers was tested without the presence of silicon nitride and its peak current gain was 70 times. From these tests and results from other programs, it is believed that silicon nitride degrades the gain characteristics of the transistor and will require further investigation to minimize this disadvantage.

3. Alignment of the Ballast and Transistor Chips

The contact mesa areas of the ballast resistor are aligned with the corresponding emitter fingers on the transistor chip by using the micropositioning equipment shown in Figure 17. This alignment is done by marking with a pencil one of the longest emitters in the repeating pattern on both the ballast resistor and the transistor chip. The ballast resistor is placed on top of the transistor with its mesas facing the emitters and the ends of the longest mesa and longest emitter approximately aligned. With the ballast resistor held by means of the vacuum chuck in the center of upper plate, final positioning is accomplished by means of the micrometer controls to bring the end of each mesa in exact alignment with the end of each emitter.

The ends of the mesas on the resistor can be seen from the opposite side of the resistor for alignment purposes because the edge of the resistor is cut at a bevel such that the ends of the mesas extend slightly beyond the circumference of the body of the resistor. The precisely aligned ballast resistor and the transistor chip are bonded together by three small dabs of silicone rubber applied between the outer edge of the resistor and the adjacent metallized surface of the transistor.

The curing time of eight hours for the silicone rubber is of some concern because it is not practical in production to take that length of time to cure each aligned assembly on the alignment fixture. Experiments were thus performed using ultraviolet light curable adhesives with cure times claimed to be less than one minute. The adhesives tried were Cauk's Nuva Seal and Nuva Fil, as well as Loctite's adhesive No. 353. However, none of these experiments were successful since the curing rate in all cases was much slower than advertised. These slow curing rates are attributed to the reflective metal surface of the transistor. Undesirable capillary penetration of these adhesives also occurred between the contacting surfaces. The standard silicone rubber adhesive does not migrate from where it is applied.

Experiments were also conducted in which the assembly was carefully removed from the fixture immediately after applying the silicone rubber. These experiments were successful if the silicone were cured for six to eight hours after removal and before attempting to assemble the emitter heat-pipe to the transistor and ballast chips.

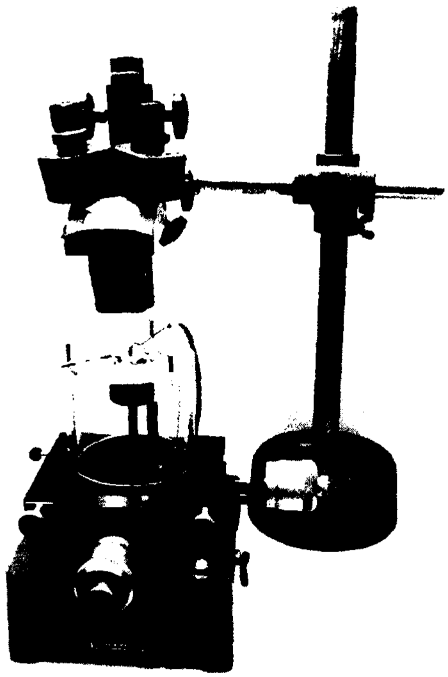


Figure 17 Micropositioning Alignment Station used to Position the Ballast Resistor on Top of the Transistor Chip.

The collector heat-pipe and transistor chip are supported by the rod surrounded by the movable table. The ballast resistor is held by the vacuum chuck in the center of the aluminum plate on top of the clear plastic cylinder. The cylinder and plate can be rotated and moved laterally along the x, y, and z axes with the micrometers. When precise alignment is achieved, the heat-pipe assembly can be raised along the z-axis (vertically) to bring the transistor chip into intimate contact with the ballast resistor. The two are then bonded together with three small dabs of silicone rubber. The microscope aids the operator in the precision alignment of the parts.

Thus, it may be possible in production to utilize the alignment fixtures for additional chips while the silicone curing occurs in a remote location.

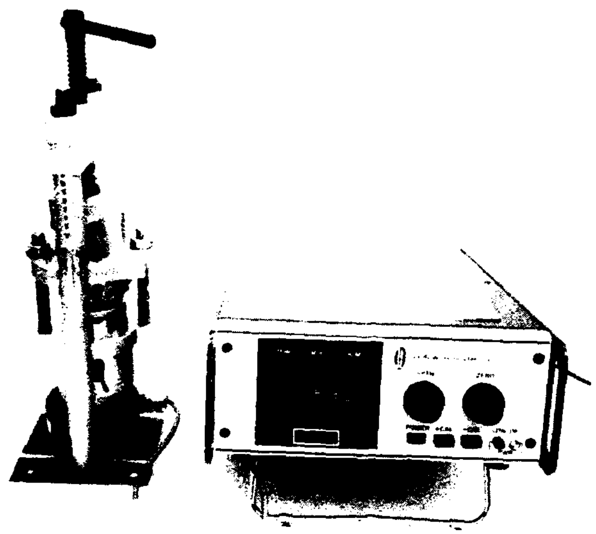
The marking of the longest emitter finger on the transistor chip and the longest mesa on the ballast resistor will not be necessary in assembling later devices. When the new masks were designed, as described above, a figurative alignment mark at the end of one of the long emitter fingers was incorporated into the mask pattern. This mark is transferred to the metallizing when the metallization patterns are defined by the photo resist exposure operation. A similar mark will be applied to the side of the ballast resistor opposite one of the longest mesas.

4. Final Assembly Clamping

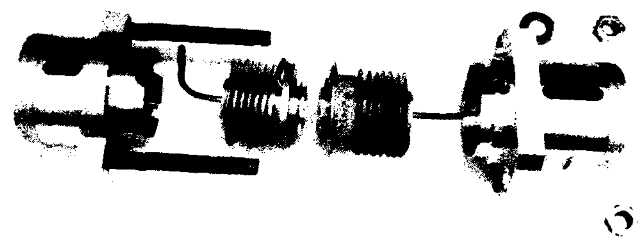
Final assembly is accomplished by slipping a weld ring over the anode heat-pipe and by placing the emitter heat-pipe on top of the collector heat-pipe subassembly in the fixture illustrated in Figure 18. The screw at the top of the fixture in the (a) part of the figure is used to apply pressure to the flanges on each heat-pipe. The load cell at the bottom of the fixture measures the applied load and displays the value on the adjacent digital instrument. The transistor is tack welded in the fixture and is completely welded in the same welding fixture as used to weld the thyristor. The tack welds are strong enough that there is little or no loss of load when the transistor is removed from the fixture.

Part (b) of the figure shows an exploded view of the final transistor assembly before clamping.

This clamping fixture is a significant improvement over the techniques used to assemble the experimental R & D contract devices. The experimental devices were fabricated by applying the load to the ends of the heat-pipe. The latter procedure caused a large percentage of transistor chips to be broken and a portion of the loading was subsequently relieved after welding by the deflection of the weld flanges when the device was removed from the fixture. By applying the load (clamping force) to the flanges in the present procedure, the chip is not overstressed and very little of the loading is relieved after welding.



(a)



(b)

Figure 18 Clamping Fixture used in Clamping the Transistor Final Assembly.

(a) Shows a transistor clamped. The load is applied by the screw at the top and is transferred to the nuts and bolts at the center prior to welding. The meter at the right displays the load measuredby the load cell at the bottom of the fixture.

(b) Shows how the heat-pipe subassemblies are assembled in the fixture prior to loading.

The load cell is also an improvement. In the fixture used to fabricate the experimental devices the magnitude of the load was measured by the deflection of a spring. Although the stress deflection curve of the spring was calibrated, its accuracy was limited by the lack of precision with which the deflection of the spring could be measured.

Experiments were also conducted on the electrical characteristics of the transistor versus the load applied. In Figure 19 the collector current, I_C, measured at two different V_{CE} values is plotted versus the clamping force. These data indicate that above 145 pounds, there is very little further gain in the collector current.

In Figure 20 is a plot of the emitter series resistance versus the clamping force. In all cases, the resistance decreases with increasing loads. However, when a load of 176 pounds was applied and let stand for five minutes, the load measured by the load cell decreased to 170 pounds and the resistance increased from 3.22 milliohms to 3.73 milliohms. It was concluded that yielding of the metals was occurring and that greater loads would neither be retained nor practical.

5. Base Lead Connection

The internal base lead for the engineering samples is soldered to the base ring on the transistor chip. This is a critical operation because there is a danger of introducing solder flux into the high voltage chamber of the device. Migration of such a contaminant could conceivably reduce the blocking voltage of the device.

It is because of this risk that the assembly procedure for later devices will be changed to that shown in Figure 13, above (Dwg. No. B3025856). A spring contact will make a mechanical connection between the base feed-through ring and the base ring. The connection will be made when the emitter heat-pipe is assembled on top of the anode heat-pipe subassembly. Thus a critical soldering operation has been eliminated. The internal spring contact is also beneficial because it has a smaller electrical impedance than the wire lead used in assembling the engineering samples.

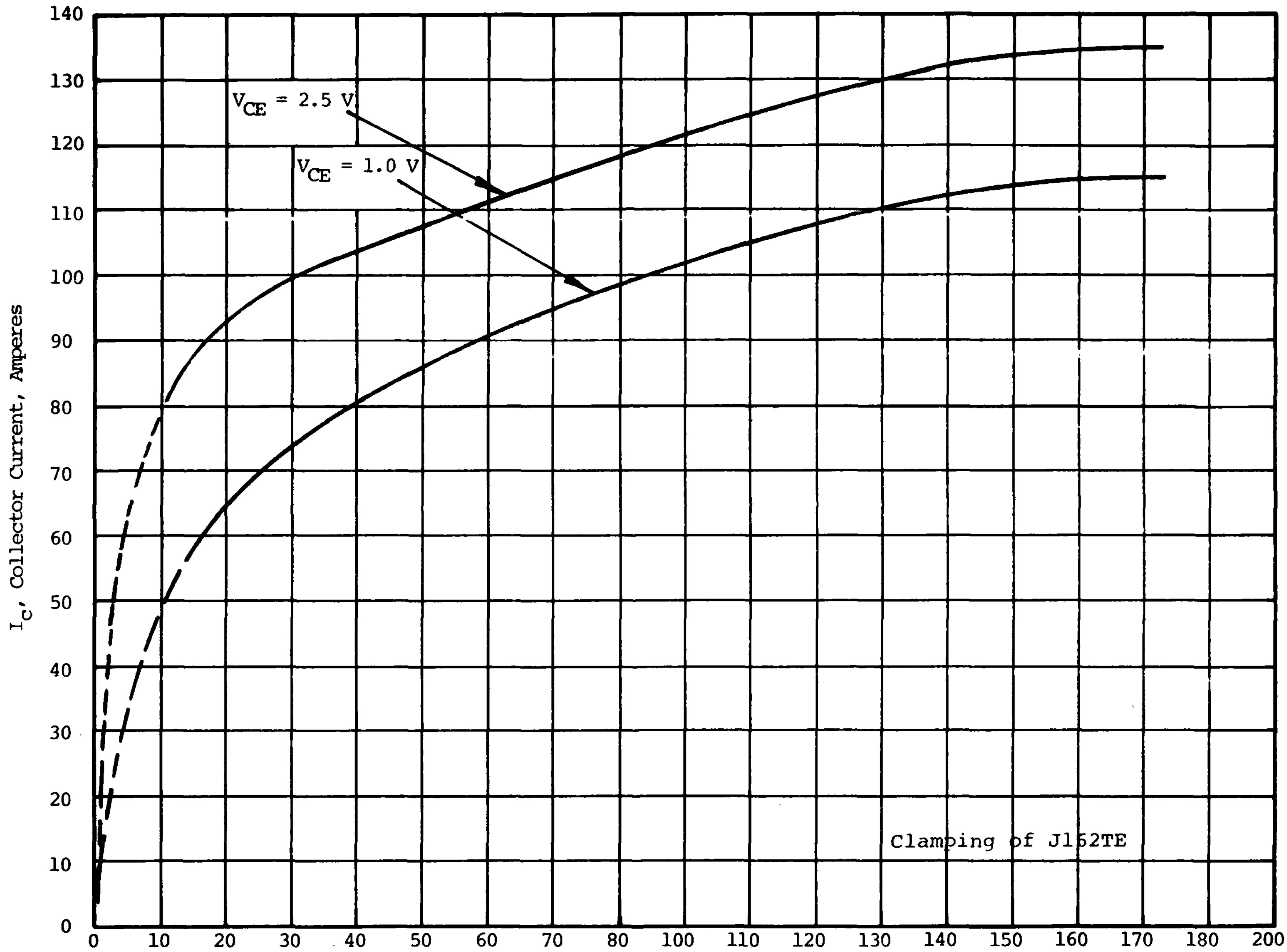


Figure 19 Change in Collector Current, I_C Versus the Clamping Force Measure at Two Different Collector-to-Emitter Voltages, V_{CE}

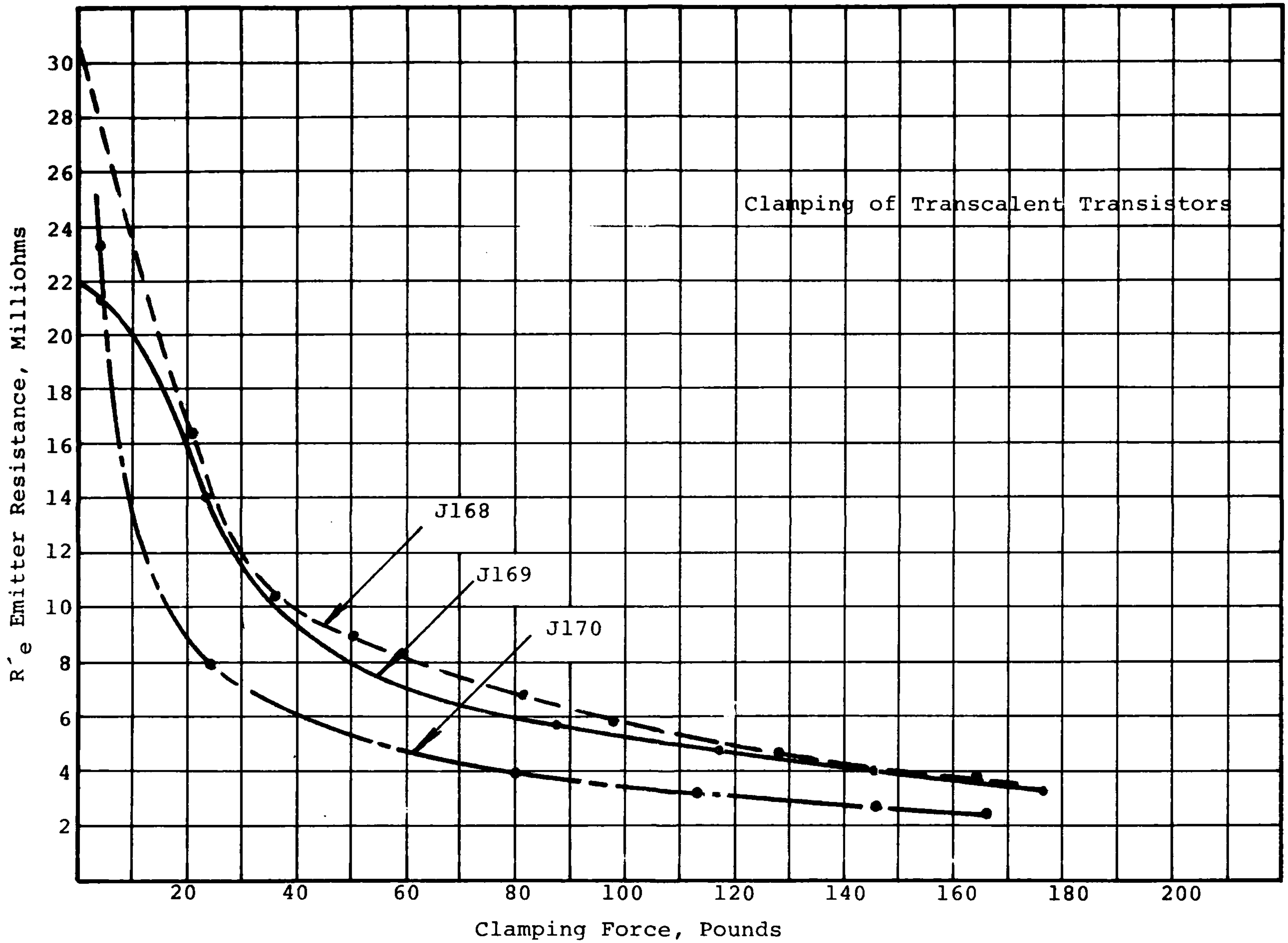


Figure 20 Change in Emitter Resistance, R'_e, Versus the Clamping Force for Three Different Transistors

6. Heliarc Welding

The two flanges attached to the heat-pipes are tack welded to the weld ring while the transistor is mechanically clamped in the fixture shown in Figure 18. The tacks are about 3/8 inch long and are strong enough to support the tensile load which is applied to them when the transistor is removed from the clamping fixture. Once the transistor is removed from the clamping fixture, a continuous weld is made at both flanges forming the vacuum-tight center chamber which protects the transistor chip, the ballast resistor, the base connection and the critical interfaces to the two heat-pipes.

The anode weld flange and the weld ring will be combined into one part for later devices. This feature can be noted in Figure 13. When this new part is brazed onto the heat-pipe, its position is such that there will be approximately a 15 mils gap between the emitter flange and the collector flange at zero load. This gap will be closed when the full clamping force is applied to the transistor.

The new weld design lends itself also to projection welding in which the loading of the transistor and the welding can be combined into one operation. Projection welding is a branch of spot welding in which a projection on a part is deformed and welded to another part when heated by its own electrical resistance.

Figure 21 shows the deflection of the present flange assembly on the emitter heat-pipe versus the loading. The sum of the deflections of the collector and emitter heat-pipe flanges at 165 pounds is the exact dimension of the gap prior to welding.

7. Exhaust Processing

The final processing of the Transcalent transistor is the same as for a Transcalent thyristor or rectifier. The center chamber is exhausted on a high vacuum system, baked at 175°C for more thorough degassing, and back-filled with dry nitrogen gas. The heat-pipes are exhausted on another vacuum system and sufficient high purity water is admitted to each heat-pipe to just fill the pores of the wick. Each of the three chambers is pinched off from the vacuum system by a cold weld process that retains the back-filled atmosphere's reliability for thousands of hours of operation.

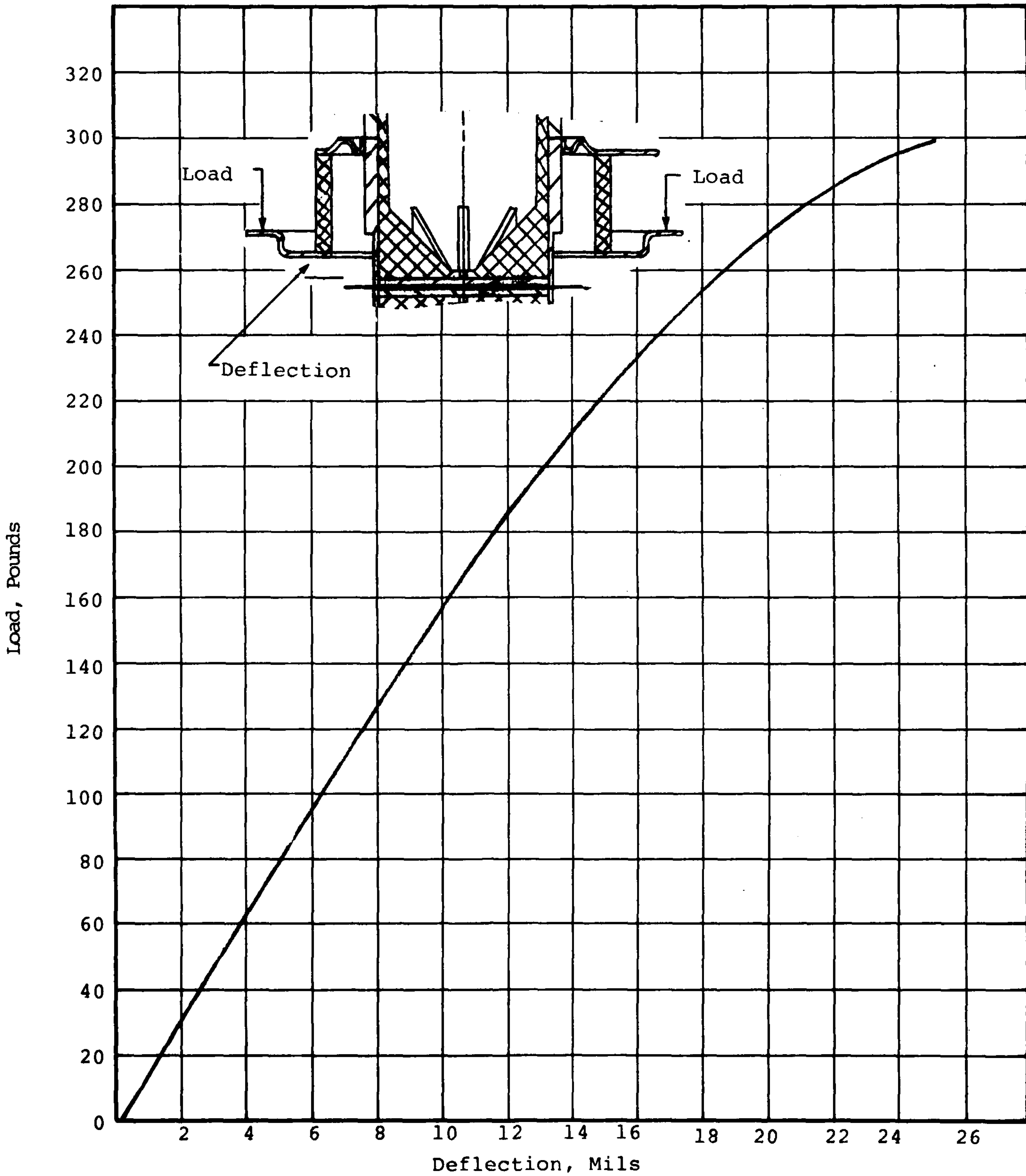


Figure 21 Deflection of the Cathode Flange Assembled Versus Loading

8. Finishing Operation

Assembled with hollow mounting studs, to allow the long exhaust tubes to extend through them, the completed transistor is next characterized using a commercial Tektronix type 576 curve tracer. These tests establish the device's gain, V_{CBO}, V_{CEO} and V_{EBO}. The thermal impedance is also measured at this point using a separate test set. Acceptable transistors next have their exhaust tubes pinched off to the proper length and the hollow mounting studs replaced with solid ones.

On completion of the above steps and the electrical tests the transistor is electroplated with nickel and conformal coated to protect the surfaces from corrosion and to improve the reduced barometric pressure operation. A label including the manufacturer's identification, the device number and the serial number is attached to each transistor prior to the conformal coating.

The last items added are the base and auxiliary emitter leads.

IV. ELECTRICAL, MECHANICAL, THERMAL AND ENVIRONMENTAL INSPECTIONS, ENGINEERING SAMPLES

A. Introduction

Several engineering sample devices were fabricated for the collection of engineering data. With these samples, the method of test and the device performance were closely compared to the limits imposed by the specifications, TABLES I, II and III, of this contract, Attachment No. 2. Performances were evaluated over a wide range of ambient temperatures from -25°C to +125°C. At the conclusion of this effort, some new limits and new test parameters were recommended.

Ten sample devices were actually assembled and the data for all of the devices is included in this report for statistical purposes. Six devices completed and passed all tests and of these, five were shipped as the Engineering Samples designated type J15381E. Data for the failed devices was utilized up to the time of failure.

The engineering samples, which were delivered to the Government, as required in "Part II, Section E, Supplies/Services and Prices" of the contract, passed the following minimum electrical performance tests:

Table I, Subgroup 1	Visual and Mechanical Inspection Physical Dimensions
Table I, Subgroup 2	Collector to Emitter Cutoff Current with Base Reverse Biased Collector to Emitter Cutoff Current with Base Open Collector to Base Cutoff Current Breakdown Voltage, Emitter to Base Forward Current Transfer Ratio
Table I, Subgroup 3	Thermal Resistance
Table II, Subgroup 1	Forward Current Transfer Ratio Saturation Voltage and Resistance

B. Table I - Group A Inspections

1. Subgroup 1 - External Characteristics

a. Visual and Mechanical Examination

All of the Transcalent transistors were visually and mechanically inspected in conformance to Method 2071 of MIL-STD-750B and Figure 1 of the Specification.

b. Physical Dimensions

The dimensions of each device were measured and recorded to verify values of Figure 1 of the Specification, using Method 2066. TABLE 9 lists the results of these measurements and TABLE 10 lists the statistical analysis. As a result of these tests and measurements made on similarly configured devices of prior contracts[1], only one change will be necessary for the base line dimension. Dimension D should be 1.910 inches maximum instead of 1.857 inches maximum as specified in the contract. Figure 22 illustrates a mechanical guage for the transistor. A fit into the gauge implies that maximum dimensions have been complied with.

2. Subgroup 2 - Electrical Characteristics at $T_A = 25 \pm 3^oC$

This series of tests is initially listed in TABLE I and is subsequently utilized as a post-test evaluation of the electrical integrity of each device after performing the inspections of TABLES II and III. Therefore, more than usual care was taken to insure the accuracy of these readings. Photographs of the initial curve tracer displays were taken and the later measurements were then compared to these photographs.

These readings are grouped by parameter, in the order taken, in Tables 11 through 15. The readings were recorded using a Tektronix Type 576 curve tracer with the connection configurations in the form of Methods 3041.1, 3036.1, 3026.1 and 3076.1 of MIL-STD-750B. The values recorded are either the highest values of voltage obtained and the current reading at that point or the value of the current reading at the voltage noted in the Specification, whichever was the most pessimistic. The failures of devices J163, J164 and J167 will be discussed in the section describing that test in which the failure occurred.

a. Collector-to-Emitter Cutoff Current with Base Reverse Biased, I_{CEV}

TABLE 11 lists the data for this room temperature parameter. The Specification allows a maximum of 15 mA leakage current at a voltage of at least 750 volts. The maximum current measured was 2.8 mA at voltages up to 900 volts just prior to avalanche. A reverse bias of one

[1]Silicon Transcalent Thyristor MM&T Contract No. DAAB07-76-C-8120 and Silicon Transcalent Rectifier MM&T Contract No. DAAK70-78-C-0120

TABLE 9

MEASURED PHYSICAL DIMENSIONS

Device Serial No. / Dimension	J159	J160	J161	J162	J163	J164	J167	J168	J169	J170
A	4.77	4.76	4.76	4.76	4.78	4.74	4.77	4.76	4.79	4.77
B	3.46	3.46	3.47	3.45	3.46	3.45	3.46	3.46	3.46	3.46
C	0.658	0.652	0.648	0.644	0.651	0.640	0.647	0.650	0.650	0.637
D	1.840	1.778	1.810	1.791	1.792	1.810	1.824	1.810	1.827	1.807
F	2.102	2.100	2.103	2.102	2.100	2.102	2.100	2.101	2.103	2.101

NOTE: Refer to Figure 1 of either the contract specification or this report for the location of each dimension.

TABLE 10

J15381E STATISTICAL ANALYSIS OF PHYSICAL DIMENSIONS

Sample Size: 10 (Units Measured in Inches)

		Dimension A	Dimension B	Dimension C	Dimension D	Dimension F
Spec Limits:	max.	5.02	--	--	1.857*	--
(Per Fig. 1 of Contract Spec.)	nom.	--	3.45	0.650	--	2.250*
	min.	--	--	--	--	--
Recorded Values:	max.	4.79	3.47	0.658	1.840	2.103
	min.	4.74	3.45	0.637	1.778	2.100
Analysis:	$\bar{x}$	4.77	3.46	0.648	1.809	2.101
	σ	0.014	0.006	0.0062	0.0185	0.0012
	3σ	0.042	0.018	0.0186	0.0555	0.0036
	$\bar{x} + 3\sigma$	4.81	3.48	0.667	1.865	2.105
	$\bar{x} - 3\sigma$	4.73	3.44	0.629	1.754	2.097
Proposed Spec. Changes:	max.	--	--	--	1.910*	2,20*
	nom.	--	--	--	--	--
	min.	--	--	--	--	--

*Figure 1 of this report reflects dimensional changes and tolerances established in the two previous MM&T contracts (refer to text). Specifically, dimension B has a ± 0.05 inch tolerance, C has a ± 0.07 inch tolerance, D is 1.91 inches maximum and F is 2.20 inches maximum. All other dimensions are as listed above.

Figure 22 Dimension Gauge

TABLE 11

COLLECTOR-TO-EMITTER CUTOFF CURRENT WITH BASE REVERSE BIASED, I_{CEV}

Inspection			Initial & Final Measurements for J15381 Serial No.										
Table	Sub-Group	Symbol	J159	J960	J161	J162	J163	J164	J167	J168	J169	J170	Units
			(Spec. Limit: I_{CEV} = 15 mA max. at V_{CE} = 750 V)										
I	2	V_{CE}	870	900	850	820	750	750	900	895	750	750	Volts
		I_{CEV}	0.09	0.16	0.03	0.01	0.70	0.90	0.30	0.07	2.5	0.50	mA
II	1	V_{CE}	870	900	860	820	750	750	--	890	740	750	
		I_{CEV}	0.08	0.15	0.03	0.01	0.60	0.90	--	0.07	2.50	0.50	
II	2	V_{CE}	870	910	860	820	750	750	--	900	760	750	
		I_{CEV}	0.07	0.16	0.04	0.01	0.70	0.90	--	0.10	3.0	0.50	
II	3	V_{CE}	865	900	850	820	750	750	--	890	750	750	
		I_{CEV}	0.20	0.16	0.05	0.04	0.52	1.00	--	0.10	2.60	0.52	
II	4	V_{CE}	865	900	850	810	720	750	--	890	750	750	
		I_{CEV}	0.05	0.12	0.02	0.01	0.40	1.00	--	0.11	2.80	0.51	
III	2	V_{CE}	880	900	855	810	--	--	--	880	750	750	
		I_{CEV}	0.04	0.10	0.03	0.01	--	--	--	0.20	2.8	0.50	
III	3	V_{CE}	880	900	850	850	--	--	--	890	750	750	
		I_{CEV}	0.03	0.03	0.03	0.03	--	--	--	0.25	2.8	0.50	
III	4	V_{CE}	880	900	850	815	--	--	--	890	750	750	
		I_{CEV}	0.06	0.03	0.02	0.01	--	--	--	0.25	2.6	0.50	
III	5	V_{CE}	880	895	850	810	--	--	--	880	750	750	
		I_{CEV}	0.02	0.03	0.02	0.01	--	--	--	0.20	2.7	0.50	

and one-half volts (negative) was applied between the base and the emitter terminals.

b. Collector-to-Emitter Cutoff Current with Base Open, I_{CEO}

TABLE 12 lists the results of this measurement. The Specification shows a 20 mA maximum current at 350 volts or more. The highest voltage achieved was 500 volts and the highest leakage current was 10 mA (at a V_{CE} = 380 V).

This test is more meaningful if described in terms of the sustaining voltage, $V_{CEO(sus)}$, and an established minimum collector current for these conditions. Since the V-I characteristic curve describes a negative resistance region immediately after breakover, difficulty is usually encountered using a curve-tracer at high currents (or with nearly vertical load lines). It is recommended, therefore, that this test be replaced with test method 3053 for an NPN device. In this case the details to be specified are: $R_{BB} = \infty$, V_{BB1} = 0 to 10 volts, Load Condition C. By experimentation L = 10 mHy, R of inductor = 0.11 ohm and R_S = 0.196 ohm.

This alternate test circuit was evaluated using devices No. J162 and J170. The V_{CC} voltage was set to 8 volts and V_{BB1} adjusted, with the base switch closed, for some small collector current. When this switch is opened, the oscilloscope trace was observed for the characteristic inductive voltage swing, collector-to-emitter. Since the traverse of the switching locus is reversed from that of the curve-tracer the negative resistance region between the $V_{CEO(sus)}$ point and the breakover voltage point is of little consequence. The inductive energy is nearly depleted at this point.

The $V_{CEO(sus)}$ for transistor No. J162 was measured at 340 volts at a collector current of 1.7 amperes. This is compared to the TABLE 12 listing of 350 volts at 0.004 amperes. The pulse width of this voltage excursion was noted at 25 microseconds.

The $V_{CEO(sus)}$ for transistor No. J170 measured at 1, 2 and 3 amperes of collector current was 425 volts compared to the curve-tracer reading of 490 volts at 0.002 ampere.

TABLE 12

COLLECTOR-TO-EMITTER CUTOFF CURRENT WITH BASE OPEN, I_{CEO}

Inspection			Initial & Final Measurements for J15381 Serial No.										
Table	Sub-Group	Symbol	J159	J160	J161	J162	J163	J164	J167	J168	J169	J170	Units
			(Spec. Limit: I_{CEO} = 20 mA max. at V_{CE} = 350 V)										
I	2	V_{CE}	490	374	390	350	350	350	408	415	403	497	Volts
		I_{CEO}	2.2	7.2	8.8	3.0	2.7	4.5	4.0	3.4	2.0	2.0	mA
II	1	V_{CE}	480	380	390	350	350	350	--	425	410	500	
		I_{CEO}	2.3	7.0	9.0	3.0	3.0	5.0	--	3.0	2.0	2.0	
II	2	V_{CE}	490	380	390	350	350	370	--	425	410	500	
		I_{CEO}	3.0	7.0	9.0	3.0	2.8	5.0	--	3.0	2.1	1.9	
II	3	V_{CE}	490	380	400	350	370	370	--	420	420	490	
		I_{CEO}	2.5	7.0	3.0	4.0	6.0	4.0	--	4.0	4.0	2.0	
II	4	V_{CE}	480	360	400	350	350	370	--	400	430	500	
		I_{CEO}	1.9	7.0	3.0	4.0	6.0	4.0	--	4.0	4.0	2.0	
III	2	V_{CE}	480	390	400	350	--	--	--	400	435	500	
		I_{CEO}	1.0	10.0	3.0	4.0	--	--	--	4.0	4.0	2.0	
III	3	V_{CE}	500	380	400	350	--	--	--	400	435	470	
		I_{CEO}	1.0	10.0	3.0	4.0	--	--	--	4.0	4.0	2.0	
III	4	V_{CE}	500	380	400	350	--	--	--	400	435	480	
		I_{CEO}	1.0	10.0	3.0	4.0	--	--	--	4.0	4.0	2.0	
III	5	V_{CE}	480	380	400	350	--	--	--	400	430	470	
		I_{CEO}	1.0	10.0	3.0	4.0	--	--	--	4.0	4.0	2.0	

All of the five engineering samples shipped had V_{CEO} values above 380 volts using the curve-tracer technique. All should have passed using the Method 3053, as described, at one ampere of collector current.

c. Collector-to-Base Cutoff Current, I_{CBO}

The results of this test are shown in TABLE 13. Values are very similar to those of the Collector-to-Emitter Cutoff Current with Base Reversed Biased and the same limits are imposed. The highest voltage reached was 917 volts and the highest current was 3.2 milliamperes. In general, the current measured for I_{CBO} is only slightly higher than that for the I_{CEV} measurement. It is recommended that the I_{CEV} test be deleted because the I_{CBO} test will suffice. Both tests are measured at 750 volts or higher.

d. Breakdown Voltage, Emitter-to-Base, V_{EBO}

The specification requires less than 50 mA of emitter current when applying 8 volts or more from emitter-to-base. The maximum voltage used was 21 volts and the maximum current was 6.6 mA on the devices shipped; serial Nos. J159, J160, J161, J168 and J169.

Transistor No. J170 showed degradation after the TABLE III, Subgroup 3 inspections involving thermal shock, moisture resistance and corrosion. The current on this device at 8 volts changed from less than a milliamp to 70 mA. All other parameters were unaffected. TABLE 14 lists these parameters.

e. Forward Current Transfer Ratio, h_{FE}

TABLE 15 lists this current gain parameter for the devices measured. The specification requires a minimum of 20 times in current gain at a collector-to-emitter voltage of 5 volts and a collector current of 10 amperes. The minimum value recorded was 36 times and the maximum value was 90 times. Only minor deviations occurred during the entire series of tests.

Figure No. 23 shows the relationship between the current gain, h_{FE}, and the pulsed collector current, I_C, for the initial readings of all devices measured. Note that most of the devices achieved collector currents of 150 to 200 amperes with gains greater than five times. This may well be a record for high voltage switching transistors.

TABLE 13

COLLECTOR-TO-BASE CUTOFF CURRENT, I_{CBO}

Inspection Table	Inspection Sub-Group	Symbol	J159	J160	J161	J162	J163	J164	J167	J168	J169	J170	Units
			Initial & Final Measurements for J15381 Serial No.										
			(Spec. Limit: I_{CBO} = 15 mA max. at V_{CB} = 750 V)										
I	2	V_{CB}	837	900	850	822	750	750	917	895	750	750	Volts
		I_{CBO}	0.06	0.12	0.06	0.06	0.60	0.86	0.01	0.1	3.0	0.51	mA
II	1	V_{CB}	870	900	860	820	750	750	--	890	750	750	
		I_{CBO}	0.20	0.15	0.03	0.01	0.60	0.90	--	0.04	3.0	0.50	
II	2	V_{CB}	870	9.0	860	820	750	750	--	900	750	750	
		I_{CBO}	0.08	0.16	0.04	0.03	0.71	0.90	--	0.08	3.0	0.47	
II	3	V_{CB}	850	902	850	820	750	750	--	890	750	750	
		I_{CBO}	0.20	0.10	0.04	0.04	0.50	1.00	--	0.10	3.0	0.47	
II	4	V_{CB}	870	902	850	810	720	750	--	890	750	750	
		I_{CBO}	0.05	0.13	0.02	0.01	0.38	1.00	--	0.12	3.0	0.50	
III	2	V_{CB}	880	900	855	810	--	--	--	890	750	750	
		I_{CBO}	0.06	0.12	0.04	0.02	--	--	--	0.20	3.2	0.48	
III	3	V_{CB}	880	900	850	850	--	--	--	890	750	750	
		I_{CBO}	0.03	0.05	0.04	0.04	--	--	--	0.27	3.0	0.52	
III	4	V_{CB}	880	900	850	815	--	--	--	890	750	750	
		I_{CBO}	0.09	0.05	0.03	0.02	--	--	--	0.27	3.0	0.50	
III	5	V_{CB}	870	890	850	810	--	--	--	890	750	750	
		I_{CBO}	0.02	0.07	0.02	0.02	--	--	--	0.20	3.0	0.51	

TABLE 14

BREAKDOWN VOLTAGE, EMITTER-TO-BASE, V_{EBO}

Inspections			Initial & Final Measurements for J15381 Serial No.										
Table	Sub-Group	Symbol	J159	J160	J161	J162	J163	J164	J167	J168	J169	J170	Units
			(Spec. Limit: V_{EBO} = 8 V. min. at I_E = 50 mA max.)										
I	2	V_{EBO}	20.5	13.4	18.6	8.0	11.0	13.0	16.0	8.0	8.0	10.0	Volts
		I_E	0.75	0.01	0.01	3.3	0.01	0.01	0.01	1.6	1.6	0.01	mA
II	1	V_{EBO}	21	13.5	18.0	10.0	11.0	12.8	--	8.0	10.0	18.0	
		I_E	0.10	0.01	0.01	0.06	0.01	0.01	--	1.5	1.8	.10	
II	2	V_{EBO}	20.5	13.2	18.0	17.0	11.0	13.0	--	10.0	10.0	18.0	
		I_E	0.01	0.01	0.01	0.50	0.01	0.01	--	4.8	1.9	0.12	
II	3	V_{EBO}	20.5	13.3	18.0	17.0	13.0	13.0	--	10.0	10.0	18.5	
		I_E	0.01	0.01	0.03	0.50	0.04	0.01	--	4.8	2.0	0.10	
II	4	V_{EBO}	20.4	8.0	18.0	17.0	10.9	13.0	--	10.0	10.0	18.0	
		I_E	0.01	5.0	0.01	0.50	0.01	0.01	--	2.0	1.9	0.10	
III	2	V_{EBO}	21.0	8.0	18.0	16.8	--	--	--	10.0	10.0	19.0	
		I_E	0.01	6.40	0.01	0.50	--	--	--	1.6	1.9	0.04	
III	3	V_{EBO}	20.4	8.0	18.0	16.0	--	--	--	10.0	8.0	8.0	
		I_E	0.01	6.6	0.01	0.45	--	--	--	1.65	2.0	70.0	
III	4	V_{EBO}	20.4	8.0	18.0	16.0	--	--	--	10.0	8.0	8.0	
		I_E	0.01	6.5	0.01	0.40	--	--	--	1.6	1.8	70.0	
III	5	V_{EBO}	20.3	8.0	18.0	16.0	--	--	--	10.0	10.0	8.0	
		I_E	0.01	6.4	0.01	0.40	--	--	--	1.6	3.6	70.0	

TABLE 15

FORWARD CURRENT TRANSFER RATIO, h_{FE}

Inspection			Initial & Final Measurements for J15381 Serial No.									
Table	Sub-Group	Symbol	J159	J160	J161	J162	J163	J164	J167	J168	J169	J170
			(Spec. Limit: h_{FE} = 20 times min. at i_C = 10 A and v_{ce} = 5 V)									
I	2	h_{FE}	38	69	63	64	89	61	90	90	48	48
II	1	h_{FE}	38	67	64	67	88	61	--	87	47	47
II	2	h_{FE}	39	66	64	65	87	62	--	89	47	48
II	3	h_{FE}	39	67	65	66	88	63	--	87	47	48
II	4	h_{FE}	39	67	65	65	87	63	--	88	48	48
III	2	h_{FE}	37	71	63	64	--	--	--	88	48	47
III	3	h_{FE}	37	65	62	63	--	--	--	85	46	45
III	4	h_{FE}	37	64	61	62	--	--	--	86	46	45
III	5	h_{FE}	36	72	65	67	--	--	--	75	38	42

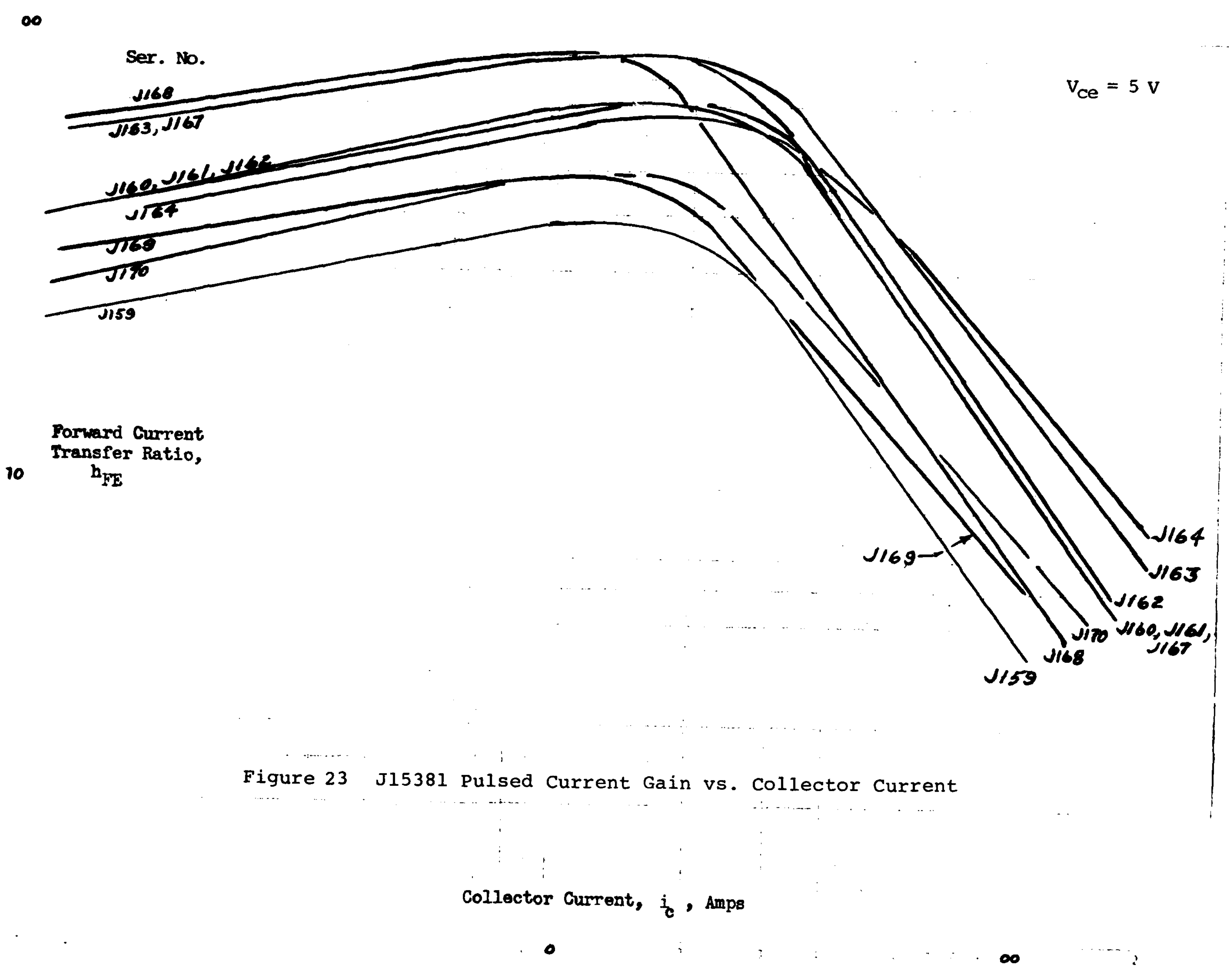


Figure 23 J15381 Pulsed Current Gain vs. Collector Current

3. Subgroup 3 - Thermal Resistance, $R_{\theta JC}$, at $T_A = 25^{\circ} \pm 3^{\circ}C$

This measurement was performed initially in TABLE I according to Method 3131.1 of MIL-STD-750B with the results tabulated in TABLE 16. This test is also listed as a final measurement in TABLE III after the tests shown for Subgroups 3 and 5. Thermal resistance was also measured after Subgroup 4 of TABLE III since the nature of this Thermal Fatigue Test and the internal construction of the device may first affect the $R_{\theta JC}$. It was thus felt prudent to take this measurement at least for information during the Engineering Phase of this contract.

The maximum value allowed by the Specification at a dissipation of 250 watts is 0.4°C/Watt and the maximum value measured was 0.18°C/Watt. A critical factor for this test is the air flow system used. By the nature of the heat-pipe operation, thermal resistance is somewhat dependent upon the air flow and the power dissipated. Figure 24 shows the range of thermal resistance measured versus the power dissipated with two cooling conditions. The air flow efficiency is dependent upon the aperture around the device being cooled.

For these tests, a standard aperture of 5.0 inches (tapered to the length of the device) by 2.8 inches (tapered to the width of the device) was used giving a 14 sq. in. or 0.0972 sq. ft. open duct. The transistor was then placed in the aperture and the air velocity measured at a distance up stream with a hot wire velcmeter. The average of three air flow measurements across the duct was 875 ft. per min. Therefore, the volumetric air flow was 875 ft. per min. times the cross section area of the duct or 85 CFM. This is well under the recommended flow of 150 CFM.

It should be noted that the temperature sensitive parameter, V_{BE}, was very well behaved for each device when compared to the junction temperature during the calibration procedure. This voltage was measured at a collector current of 0.5 ampere. The formulation generated by this procedure allows the determination of junction temperature by external measurement and is in the form of the following equation[1]:

$$T_J = A - B\ V_{BE} \qquad (1)$$

[1] Modeling the Bipolar Transistor, Ian Getreu, Equation 2.1. Tektronix, Inc. Book No. 062-2841-00

TABLE 16

THERMAL RESISTANCE, $R_{\theta JC}$

Table	Sub-Group	Symbol	J159	J160	J161	J162	J163	J164	J167	J168	J169	J170	Units
			Initial and Final Measurements for J15381 Serial No.										
			(Spec. Limit: $0.40^{\circ}C/W$ max. at I_C = 50 A and V_{ce} = 5 V)										
I	2	$R_{\theta JC}$	0.17	0.16	0.13	0.17	0.14	0.18	0.13	0.17	0.16	0.14	$^{\circ}C/Watt$
III	3	$R_{\theta JC}$	0.17	0.16	0.14	0.17	--	--	--	0.18	0.18	0.15	
III (Not Required)	4	$R_{\theta JC}$	0.16	0.12	0.13	0.16	--	--	--	0.16	0.15	0.15	
III	5	$R_{\theta JC}$	0.17	0.15	0.14	0.16	--	--	--	0.17	0.15	0.15	

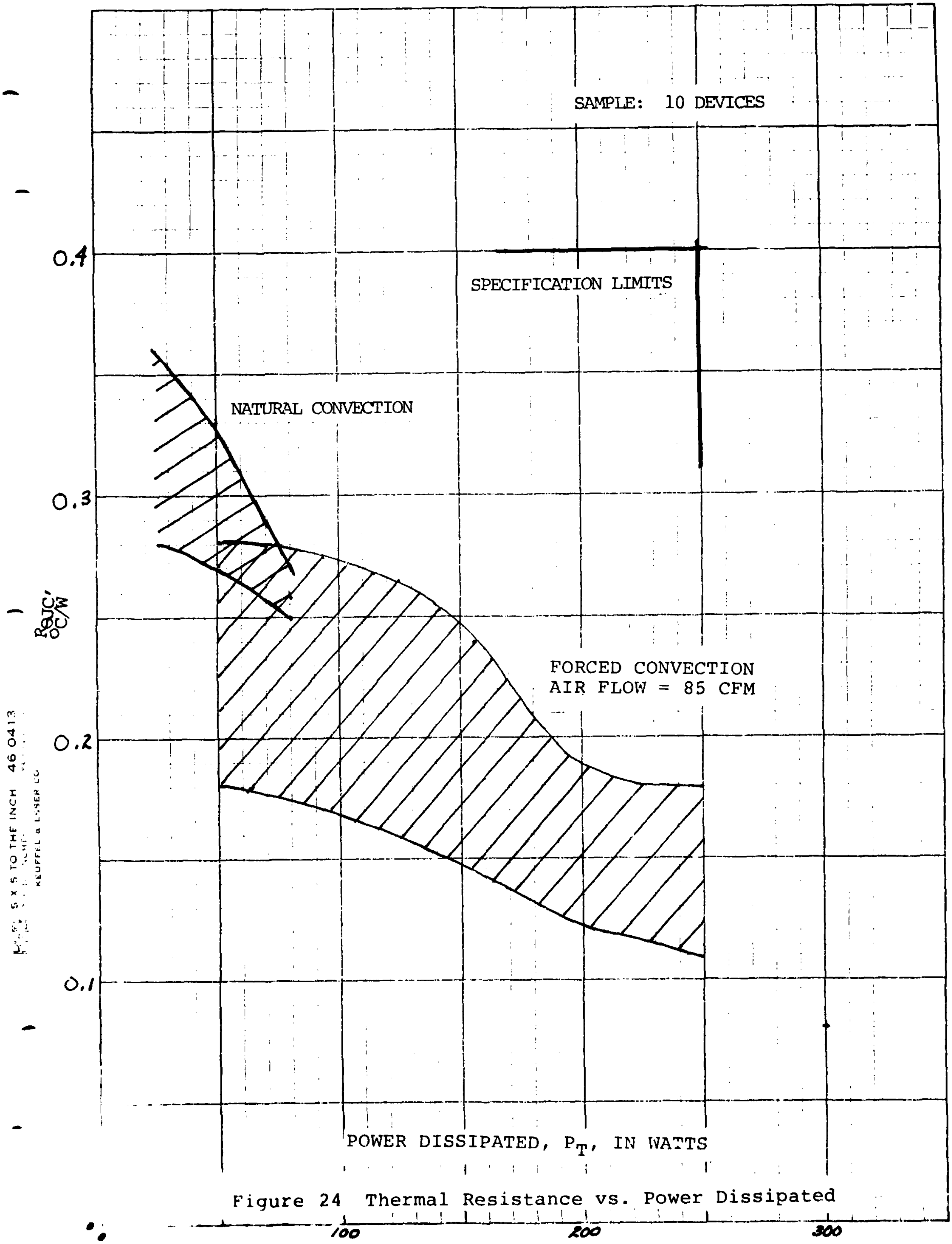


Figure 24 Thermal Resistance vs. Power Dissipated

where:

T_J = junction temperature in degrees C

The coefficients A and B are given in TABLE 17 for each device, as determined from the empirical calibration data. The linearity of this equation is derived from the formulation in reference 1.

4. Subgroup 4 - Collector-to-Emitter Cutoff Current with Base Reverse Biased, I_{CEV}, with Case Temperature = 125 ± 6°C.

   Investigation of this parameter was carried out in accordance with Method 3041.1. Voltage and current were recorded at incremental levels of temperature. Figure 25 shows these results at the final temperature of 125°C. Figure 26 shows the variation in current with temperature at a fixed applied voltage of 750 volts. As can be seen from these graphs, the only device that failed, No. J167, demonstrated a higher leakage current than the others. The slopes of J167 as well as J163 and J164 of Figure 25 are shown dashed to illustrate differentiation.

   In Figure 26, no explanation is apparent for the saturation of the leakage current at higher temperatures. As the samples get larger, significance may be attached to both this current change and to the slope of the V-I curves in Figure 25.

C. TABLE II - Group B Inspection

1. Subgroup 1 - D.C. Gain, Saturation Voltage and Dissipation at $T_A = 25° \pm 3°C$

   a. Forward-Current Transfer Ratio, h_{FE}, DC Conditions

      This parameter was measured per Method 3076.1 during the TABLE I, Subgroup 3, Thermal Resistance measurements. The base current, I_B, was recorded at a collector current, I_C, of 50 amperes and a collector voltage, V_{CE}, of 5 volts D.C. The current gain was calculated and the results are tabulated in TABLE 18 for each device. The Transfer Ratio is the actual current gain derived by dividing I_C by I_B.

TABLE 17

THERMAL COEFFICIENTS

Serial No. (Units)	A (°C)	B (°C/V)
J159	293.5	446.7
J160	294.2	447.5
J161	293.1	446.7
J162	289.5	439.9
J163	291.9	439.9
J164	288.5	440.2
J167	286.4	440.7
J168	282.9	431.2
J169	309.4	455.0
J170	300.1	444.9

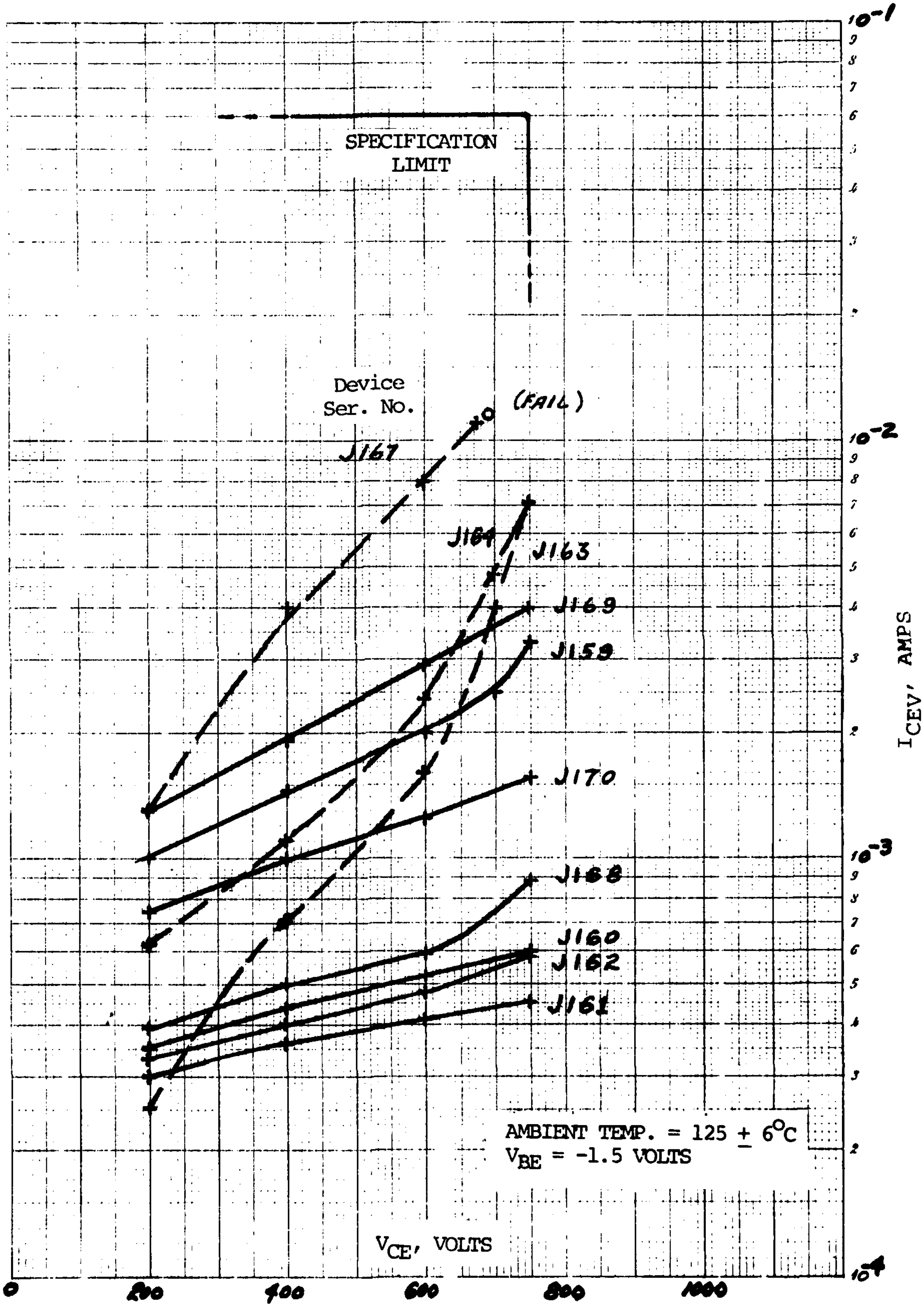


Figure 25 Collector-to-Emitter Cutoff Current with Base Reversed Biased

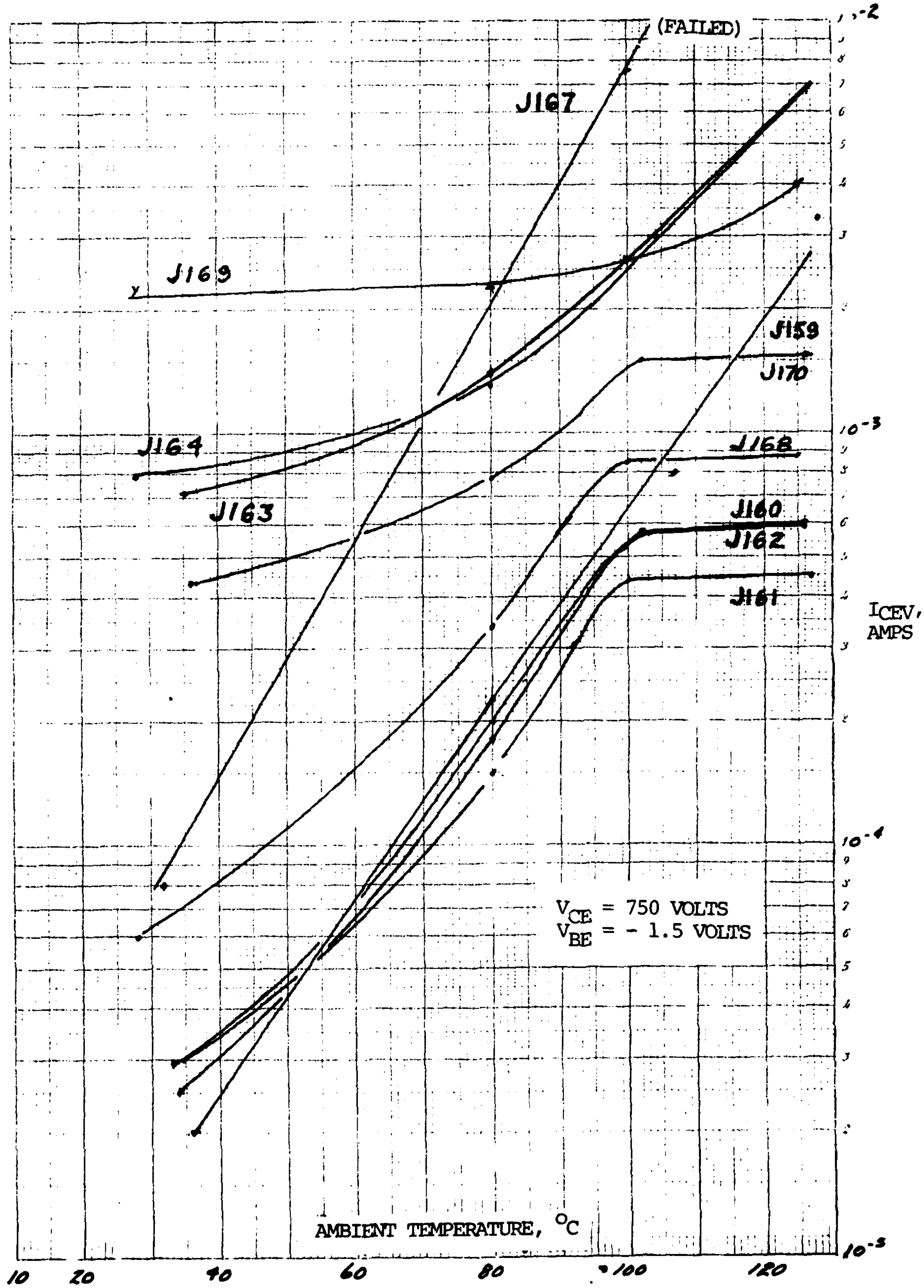


Figure 26 Collector-to-Emitter Cutoff Current with Base Reversed Biased

TABLE 18

D.C. FORWARD CURRENT TRANSFER RATIO

Device Serial No.	D.C. h_{FE}
	(Spec. Limit: 10 Times Min.)
J159	10 times
J160	16
J161	19
J162	17
J163	28
J164	31
J167	19
J168	14
J169	13
J170	14

The results of this test are referred to in a discussion in the Technical Proposal RCA DP-8165, dated 6 October 1978, page III-60, where a minimum value of six instead of ten times was suggested. A statistical analysis of this data supports the suggested revised limit of six times.

b. Saturation Voltage and Resistance, $V_{CE(sat)}$ and $r_{CE(sat)}$.

This measurement was initially taken per Method 3071 during the TABLE I, Subgroup 2 tests of the Forward Current Transfer Ratio and data for all ten devices included. The minimum value of V_{CE} at a collector current, I_C, of 50 amperes was noted along with the base drive current, I_B. The Saturation Resistance is the quotient of $V_{CE(sat)}$ and I_C. For the maximum voltage Specification of 2.0 volts this resistance calculates to be 0.04 ohm maximum.. The data is tabulated in TABLE 19.

The resulting current gain for these results is lower than for the preceeding h_{FE} test because of the greatly reduced V_{CE} value at saturation. In general, the current gain is directly proportional to the V_{CE} value used. However, this gain must be balanced against the dissipation and safe operating area values in any particular circuit.

c. Safe Operating Area (Continuous D.C.), P_T

Nine of the devices were operated per Method 3051, but modified to a common emitter connection. Four combinations of voltage and currents were used up to a V_{CE} of 20 volts and a collector current of 50 amperes such that the power dissipated by the device was in excess of 400 Watts but less than 450 Watts.

The four combinations used were 8 volts at 50 amps (400 W), 10 volts at 40 amps (400W), 13.4 volts at 30 amps (402 W), and 20 volts at 20 amperes (400 W). The cooling conditions were identical to those used for TABLE I, Subgroup 3, Thermal Resistance, namely, less than 150 CFM.

d. Final Measurements for TABLE II, Subgroup 1

Data from these measurements are found in TABLES 11 through 15 and show no major deviations from the initial readings.

TABLE 19

SATURATION CHARACTERISTICS

Serial No.	$V_{CE(sat)}$	$r_{CE(sat)}$	I_B
J159	0.60 volts	0.012 ohms	12 amps.
J160	0.42	0.008	10
J161	0.40	0.008	8
J162	0.35	0.007	8
J163	0.28	0.006	6
J164	0.28	0.006	6
J167	0.31	0.006	8
J168	0.47	0.009	8
J169	0.28	0.006	8
J170	0.21	0.004	7

2. Subgroup 2 - Switching Rates and Pulsed Collector Current at $T_A = 25^{o} \pm 3^{o}C$

a. Safe Operating Area (Switching), t_{on} and t_{off}

This test utilized the circuit of Test Method 3053 of MIL-STD-750B with the exception that precision current tranformers were used instead of a current monitoring resistor, R_s. To implement the switch in the base circuit and to reduce driver losses drastically, two power FETS were used and their connections shown in the "Transistor Pulse Driver" of Section V, Test Equipment. There were no major differences in the operation of the nine devices and, therefore, the results are summarized statistically in TABLE 20.

Tests were performed with an i_C of 50 amperes, a V_{CE} of 300 volts at a switching rate of 5,000 Hertz. Pulse durations greater than six microseconds were used with a load resistance of six ohms. The ambient temperature was $28^{o}C$ and the maximum case temperature encountered for any one device during the five minute minimum switching test was $45^{o}C$. From this data, it is concluded that the switching SOA Specification has been met.

b. Safe Operating Area (Pulsed)

This test, as specified in Method 305, is under the conditions of the type generated by the Tektronix Type 576 Curve Tracer, namely 300 µs pulse width at 0.0012 duty factor. With 20 amperes of drive, i_B, all of the devices were operated in excess of the 100 amperes of peak collector current, i_C, as listed in TABLE 21a. For purposes of a Safe Operating Area definition, the V_{CE} voltage at the i_C current is listed for each device. Also, the base current is shown in TABLE 21b for a V_{CE} of 10 volts and an i_C of 100 amperes.

c. Final Measurements for TABLE II, Subgroup 2

These measurements are found above in TABLES 11 through 15. No major deviations occurred from the initial values.

TABLE 20

J15381 TRANSISTOR SWITCHING RATES

Units	I_{b1} (Amps)	$-I_{b2}$ (Amps)	t_d (μs)	t_r (μs)	t_{on} (μs)	t_s (μs)	t_f (μs)	t_{off} (μs)
$\bar{x}$	4.97	4.62	0.12	0.56	0.74	2.5	0.487	2.99
σ	0.056	0.220	0.016	0.038	0.046	0.304	0.093	0.317
3σ	0.168	0.660	0.048	0.114	0.138	0.912	0.279	0.951
$\bar{x}$ + 3σ	5.14	5.28	0.168	0.69	0.88	3.41	0.766	3.94
$\bar{x}$ - 3σ	4.80	3.96	0.07	0.45	0.60	1.59	0.21	2.04
Spec. Limits	--	--	--	--	2.5 max.	--	--	6.0 max.

where: I_{b1} is the applied forward pulse drive current.

$-I_{b2}$ is the applied reverse pulse drive current.

t_d is the delay time.

t_r is the rise time.

t_{on} is the sum of t_d and t_r.

t_s is the storage time.

t_f is the fall time.

t_{off} is the sum of t_s and t_f.

TABLE 21

PULSED SAFE OPERATING AREA DATA

a. Constant Base Current, i_B

Serial No.	i_c (Amp.)	V_{CE} (Volts)	i_B (Amps)
(Spec. Limit: i_c = 100 A min.)			
J159	120	8.2	20
J160	148	10.0	
J161	147	10.0	
J162	150	10.0	
J163	170	9.0	
J164	181	9.2	
J168	127	7.3	
J169	125	7.8	
J170	135	7.4	20

b. Constant V_{CE} and i_c

Serial No.	i_c* (Amp.)	V_{CE} (Volts)	i_B (Amps)
J159	100	10.0	18.0
J160			8.1
J161			7.9
J162			7.8
J163			5.8
J164			5.1
J168			9.8
J169			10.0
J170	100	10.0	8.0

*Specification limit value of collector current.

3. Subgroup 3 - Safe Operating Area Forward Bias Second Breakdown, $I_{s/b}$

The Specification refers to Method 3051 of MIL-STD-750B, a Safe Operating Area Test under D.C. conditions. However, the intention of this test is to utilize the circuitry described in this method and to evaluate the J15381 transistor under high power pulsed conditions, as evidenced by the pulse conditions specified in Attachment No. 2 to the contract.

A test set was used, utilizing a circuit described on pages 55 to 57 of the Final Technical Report for MERADCOM Contract No. DAAK02-72-C-0642, "Development of a High Voltage and High Current Transcalent Transistor." The equipment is also briefly described in Section V of this report. The prominent feature of this equipment is its ability to evaluate a transistor nondestructively for the simultaneous application of high voltage and high currents for a specified duration of time. The conditions of this operation are summarized below:

V_{CC} (Volts)	i_C (Amps)	Pulse Duration (μSec.)	No. of Pulses
200	10	100	5
100	1	10,000	5

Each of the nine devices was subjected to at least three pulses of each type at the above conditions maintaining one minute off between pulses. No cooling air was applied during these tests. The Safe Operating Area Forward Bias Second breakdown test as previously listed in the specification is adequate. All the engineering devices met this requirement.

a. Final Measurements for TABLE II, Subgroup 3

A repeat of Subgroup 2 of TABLE I was performed and the results are shown above in TABLES 11 through 15.

4. Subgroup 4 - Reverse Bias Second Breakdown, $E_{s/b}$

A problem became apparent when the circuitry for Subgroup 4, Reverse Bias Second Breakdown was being assembled and tested. Since the voltage across an inductor is given by the inductance in Henries times the rate of change of the current through the inductor, it became apparent that in order to reach a collector current of 10 amperes in a 300 µsec interval with a 10 milliHenry inductance the voltage required is over 300 volts! Since the specification lists a voltage condition of 10 volts, one of the test parameters had to be altered. Under consideration in the design of this experiment is the energy stored in the inductance and the resulting voltage transient impressed on the transistor under test. Using a 48 µH inductor for an initial test, the transient voltage swing was observed for various initial current levels and pulse widths. For turn-on conditions the collector current calculated for a 300 µsec pulse width and a 10 volt source is 62.5 amperes:

$$\Delta I_C = \frac{V_{CC}}{L}(\Delta T) = \frac{10}{48 \text{ X } 10^{-6}}(300 \times 10^{-6}) = 62.5 \text{ amps.} \tag{2}$$

Then for turn-off conditions and an assumed transition time of 5 microseconds, the transient voltage swing may be estimated by the calculation below.

$$V = L\frac{\Delta I_C}{\Delta T} = (48 \times 10^{-6})\frac{62.5}{5 \times 10^{-6}} = 600 \text{ volts} \tag{3}$$

The objective in a Reverse Bias Power Test is to allow this induced voltage to rise to the $V_{CEV(sus)}$ level while the collector current decays toward zero. Thus power is dissipated while the base-emitter junction is reverse-biased. The conditions of voltage and current that were reached in this test with the revised test parameters more nearly approach the actual operating voltage and current for this device. The circuit of MIL-STD-750B, Method 3053 was compiled with using the inductive load (load condition C). The R of the 48 microHenry inductor used was 0.048 ohms. Thus, for a test frequency of 100 Hz, the Q of the inductor may be calculated:

$$Q_L = \frac{WL}{R} = \frac{(2\ \pi\ 1000)\ (48 \times 10^{-6})}{0.048} = 6.3 \tag{4}$$

The test specification refers to an inductor with a Q in excess of 100 for a 10 mHy value. The Q of the smaller inductor should, therefore, be specified at a smaller value and it is recommended that a Q greater than 5 be used.

TABLE 22 shows the results of these tests for the nine transistors tested. The collector current at the end of the 300 microsecond turn-on period is listed in the second column. The limiting voltage, actually $V_{CEV(sus)}$, is listed in the third column. The limiting voltage, actually $V_{CEV(sus)}$, along with the pulse width measured at the 50% points are listed in the third and fourth columns. The last column of TABLE 22 lists the highest value of current reached during the initial flat-top region of the voltage pulse. This current ramps to zero during this voltage excursion and, of course, represents dissipation. For all devices, the voltage swing at turn-off was reproducible and contained no inconsistencies that indicate instabilities or reasons for rejection. It is therefore recommended that the Specification be altered from an inductance of 10 mHy to 48 μHy and a Q from greater than 100 to a Q greater than 5. Also the collector current should be changed from 10 amperes to 50 amperes. Other values should remain, as is, in the Specification.

a. Final Measurement of TABLE II, Subgroup 4 Test

The repeat of Subgroup 2 of TABLE I showed little alteration of the device characteristics as shown above in TABLES 11 through 15 of this report.

D. TABLE III - Group C Inspection

1. Subgroup 1 - Barometric Pressure (Reduced) at T_A = $25^{\circ} \pm 3^{\circ}C$

a. Test Results

Each of the nine transistors was prepared for this test by being labeled and given an application of conformal coating. Experience with a thyristor of this Transcalent configuration in the prior MM&T Contract revealed that the use of this coating prevented corona at the high voltage insulator specifically at the base pin area.

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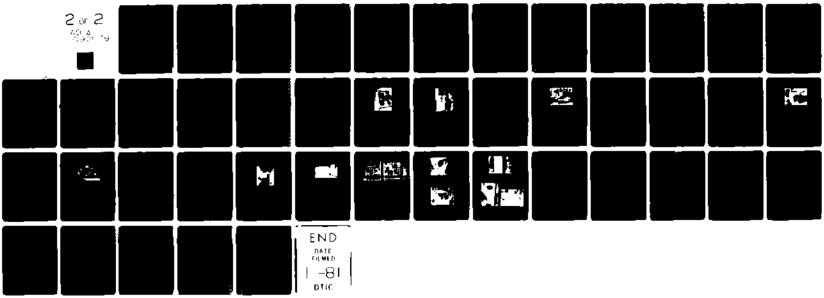

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TABLE 22

REVERSE BIAS SECOND BREAKDOWN TEST RESULTS

Serial No.	I_C (D.C. Amps)	V_{CE} (Peak Voltage Swing)	Pulse Width @50% Pts. (μsec.)	I_C @ V_{CE} (Peak) (Amps)
J159	60	510	8	48
J160	70	540	11	54
J161	70	562	11	50
J162	71	530	11	57
J163	74	450	12	56
J164	70	505	11	55
J168	60	550	7	46
J169	60	555	8	44
J170	56	525	7	45

Test Method 1001.1 was used at a peak voltage value of 750 v, a reduced pressure of 15 mm of Hg with the base reverse biased at a negative 1.5 volts. Using a 60 Hz half-wave power supply, no corona was observed for the test duration of one minute for each device.

b. Final Measurements

Final measurements were not required but an engineering test of V_{CBO} indicated that this parameter remained the same for each device after the reduced barometric pressure test.

2. Subgroup 2 - Breakdown Voltage Life Test at $T_C = 125 \pm 6^oC$

a. Test Results

This test was to be performed in accordance with the method described in paragraph No. 4.6.1 of Attachment No. 2 to the contract. The test conditions were to be a a V_{CEO} of 300 v and with the base shorted to the emitter (bias condition C) in the specified test circuit configuration (Figure 2 in Attachment No. 2) for a period of 200 hours. However, due to an error, six transistors were subjected to a V_{CEO} of 750 volts instead of the 300 volts specified at the elevated case temperature of 125 ± 6^oC and the bases were open circuited (bias condition D). The failure of two transistors, Nos. J163 and J164, resulted from this overstress.

Two observations may be made: First, that all six devices operated for at least 24 hours under these high stresses, and second, that transistors Nos. J163 and J164 both had unique slopes of V_{CEV} vs. log of I as displayed in Figure 25. After reduction of the voltage and application of the correct bias, the remaining seven devices completed the required 200 hours without incident.

It should be noted that the Specifications Detail for this test should read: "...V_{CE} = 300 V,..." instead of V_{CEO}, since the bias condition C and not D is specified.

b. Final Measurements of TABLE III, Subgroup 2

The tests of TABLE I, Subgroup 2 were repeated as shown in TABLES 11 through 15 of this report. No change occurred in the characteristics of the remaining seven transistors.

3. Subgroup 3 - Environmental Atmosphere Tests

a. Thermal Shock (Temperature Cycling)

This is the first of a sequence of three environmental tests and consists of five cycles (Test Condition B) of a temperature excursion between 125°C and the lower value of -25°C. Test Method 1051.1 of Mil-STD-750B refers to Method 107D of MIL-STD-202E for this test.

b. Moisture Resistance

This test consists of ten consecutive cycles between an ambient temperature of 25 and 65°C at a relative humidity ranging between 80 and 98% as specified in Method 1021.1 of MIL-STD-750B which, in turn, refers to Figure 106-1 of Method 106D, MIL-STD-202E. The initial conditioning is to be omitted according to the Specification.

c. Salt Atmosphere (Corrosion)

This test, in accordance with Method 1041.1 MIL-STD-750B, is to simulate the effects of salt fog atmosphere on the transistors. At the completion of this test, the devices were washed and brushed off. There was no evidence of corrosion that would interfere with the application of the device, however, there were some traces of "rust" on the weld flange of each device. This was due to an uneven application of the conformal coating. In production, the brush-on procedure for this coating should be replaced with spray techniques for more uniform coverage.

d. Final Measurements of TABLE III, Subgroup 3

These tests include both Subgroups 2 and 3 of the TABLE I Specification. Subgroup 2 test results are shown in TABLES 11 through 15 of this report and the Subgroup 3 test for each device is shown in TABLE 16 of this report.

TABLE 14 contains the only major change of a device characteristic and is sufficient to be called a failure. The I_E of transistor No. J170 is in excess of the specified 50 mA maximum at 8 volts of V_{EBO}. It is suspected that the Thermal Shock (Temperature Cycling) test caused the change in this characteristic. Since none of the other parameters were adversely effected, the device was subjected to the remaining tests.

4. Subgroup 4 - Thermal Fatigue Test

a. Test Results

The test conditions for this test are listed in paragraph 4.6.2 of the Specification. To implement this test, the universal test gear described in Section VIII of this report and used also for the thermal impedance and the D.C. operation of the transistors, was modified to include the contacts of a dual timer in series with the base circuit of the transistor. The timers were adjusted for two minutes on and two minutes off. The base current was adjusted to produce 50 amperes of collector current with about 2.5 volts applied from the collector-to-emitter.

The collector-to-emitter voltage was then adjusted slowly upward until the case temperature reached a value between 80 and 100°C when the power was applied for two minutes. The air flow was sufficient to reduce the case temperature to a value between 20 and 40°C during the off period. An event counter recorded the number of cycles, and an overall timer was set for 14 hours to allow unattended operation.

A strip chart temperature recorder was used to confirm the case temperature excursions and the number of cycles. A sample of the chart recorder is shown in Figure 27. Each tested transistor was operated in excess of 200 temperature cycles.

b. Final Measurements for TABLE III, Subgroup 4

In addition to the Subgroup 2, TABLE I tests, the Subgroup 3 Thermal Resistance Test was also included in the final measurements for the engineering samples. TABLES 11 through 16 list the results of these tests, and show little change from the initial measurements.

5. Subgroup 5 - Environmental Mechanical Tests

a. Shock

This and the vibration tests comprise the last subgroup of the TABLE III, Group C Inspections. Method 2016.2 of MIL-STD-750B was used for the non-operating shock test. The shock test requires five blows of 500 G at 1 millisec. duration in each of the X_1, Z_1, and Y_1 orientations. The orientations are described in

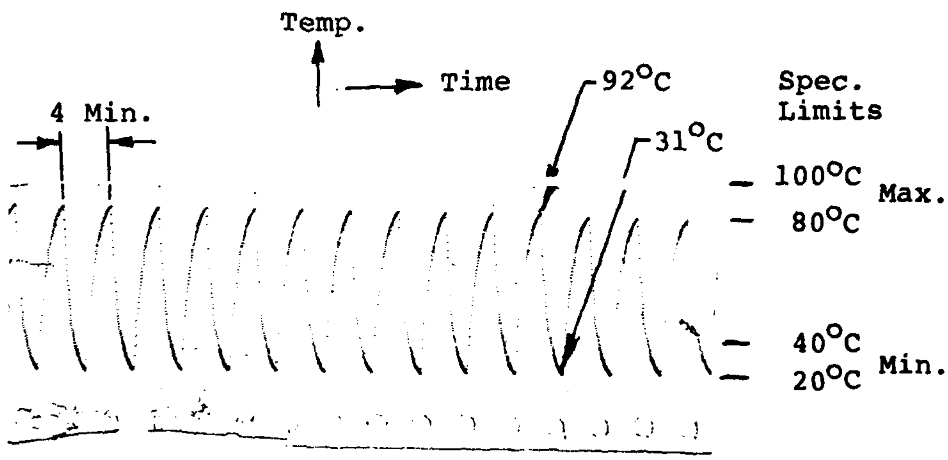


Figure 27 Thermal Fatigue Temperature Cycle Chart

Section 4. 2 of MIL-STD-750B.

b. Vibration

Method 2056 was used at an amplitude of 5 G over a frequency range of 100 to 1,000 Hertz with the wire leads removed from the devices.

c. Final Measurements for TABLE III, Subgroup 5

TABLES 11 through 16 list the results of the final electrical and thermal tests given to the devices. Except for the I_{EB} of transistor No. J170, the only other parameter to change significantly was measurement of the Forward Current Transfer Ratio for transistors Nos. J168 and J169. Transistor No. J168 showed a 14% decrease and transistor No. J169 showed a 19% decrease but both are still within the specification limits.

V. ADDITIONAL TESTS FOR TRANSISTOR IMPROVEMENT

During the course of manufacture, questions arose over parameters that may be used for control purposes and the best usage of each. Therefore, to further characterize the transistor, some parameters were studied as a prelude to the assembly of a large number of devices. These experiments ranged from Transistor Modeling to parallel operation of switching transistors. In some cases, no conclusions were drawn because of the small sample involved.

A. Transistor Modeling

Transistor studies by others have evolved into a rather sophisticated form with the objective to resolve a given device to a simplified model that can easily be handled by a computer program. This is useful to predict the transistor's performance in a given circuit. To this end, certain parameters of the device must be measured. Guidance for these measurements and for the model of the transistor was derived from a 1976 Tektronix, Inc. publication entitled "Modeling the Bipolar Transistor" by Ian Getreu. A particular model was not selected nor was the computer program for the final system. Some of the parameters measured were as follows:

1. The forward common-emitter large-signal current gain is defined in the normal active region of the device. In actuality peak values of gain were used which occur at collector currents from 10 to 25 amperes. The transistor gain ranged from 20 to 180 from device to device and it was found the high current gain was influenced inversely. Therefore a nominal value of 50 to 60 times is desired.

2. Transistor saturation current is useful in device definition and is easily measured. Typical values range from 2.2×10^{-10} to 4.6×10^{-11} amperes. Since this parameter is directly proportional to the active emitter-base junction area, its value may be readily understood.

3. Resistance between the emitter terminal and the active emitter region which in the case of the Transcalent Transistor includes the ballast resistor wafer placed between the transistor emitter contacts and the emitter heat-pipe. Measurements were made with sensors near the

ceramic insulator although the heat-pipe produces little error because of its low ohmic value. Typical values for the emitter resistance range from eight milli-ohms for the tungsten ballast resistor to eleven milli-ohms for a ballast made from silicon. The measurements have also been substantiated in devices with much larger areas where results follow standard resistance formulation.

4. The transistor unity gain bandwidth was measured using the facilities at the RCA Princeton Laboratories, N.J. The results were recorded at a pulsed operating level of one ampere of collector current at 20 volts. With a sample of five devices, the unity gain bandwidth ranged from 1.4 to 2.0 MHz.

5. Attempts to measure other parameters were made but the results were unclear. Notably among these were the measurements of junction capacitances and the resistance between the base terminal and the active base region. These particularly are necessary in the computer modeling of the transistor structure.

B. High Frequency Operation, Resistive Load

Experiments were conducted using transistors with the silicon configuration identical to the J15381 but with larger fins on the heat-pipes. A conventional driver using a single 20 ampere bipolar transistor and a bias supply supplied through a four ohm resistor was used initially. Frequency and power levels were limited by the driver. The second group of data was recorded using complementary power Darlington transistors reducing the power dissipated in the driver and also resulted in an approximate four to one reduction in storage time of the Transcalent Transistor. This driver had the disadvantage of circuit complexity and extra power supplies. The final group of data was recorded using the power FET devices recently introduced to the market. The circuit, described in Section VIII under Test Equipment Description has the advantage of a single power supply and only minor storage times associated with the driver itself. It also combines complementary operation with overdrive techniques which is enhanced as the frequency is increased. The circuit now had limitations in the collector load as it became difficult to reduce the inductance in this circuit. Computer grade capacitors were used but were still not adequate for transistor evaluation beyond the levels shown in Table 23. The circuit could not be safely operated without snubbers.

TABLE 23

HIGH FREQUENCY SWITCHING DATA

(Resistive Load)

Freq. KHz	V_{CE} Volts	I_C Peak Amperes	I_C Av. Amperes	Peak Load Power Watts	Av. Load Power Watts	Duty Factor
NOTE 1:						
5	350	50	2.5	17500	875	.05
11	350	49	2.22	17150	777	.045
33	350	45.9	3.15	16065	1100	.07
50	350	43	4.7	15050	1645	.11
NOTE 2:						
30	350	24.1	12	8435	4200	.50
50	300	24	11	7200	3300	.46
NOTE 3:						
40	330	36.5	15.4	12045	5082	.42
50	325	38	19.5	12350	6338	.51
500	56	5	2.5	280	140	.5

NOTE 1: Single Bipolar transistor driver; bias supplied through four OHM resistor.

NOTE 2: Driver used complementary pair, bipolar transistors.

NOTE 3: Driver used Power FETs in complementary configuration.

C. Paralleling Transistors

For applications requiring higher current levels and excluding availability of larger devices, paralleling of transistors is required. Current sharing among the transistors used may be realized by careful selection of devices with nearly identical switching parameters. This is not practical since on replacement of an individual device the selection process must be repeated. However, with proper emitter ballasting and a driver with fast switching capabilities differences in transistor parameter may be de-emphasized.

Emitter ballasting for each device was attempted by inserting a small annular ring of carborundum material between the emitter heat-pipe and the terminal bus. A ring about 1/8 inch thick measured 90 milli-ohms and was sufficient to provide total collector currents to 80 amperes with a 14% unbalance in current sharing. The problem of non-coincident turn-off due to variations in storage time was not addressed until the power FET driver was developed. Even then the driver capability was not able to operate more than one device efficiently. The desired combination of emitter ballasting and a power FET driver with more output was not tried.

VI. ELECTRICAL AND THERMAL INSPECTIONS OF THE ADDITIONAL DEVICES

A. Introduction

As a requirement of the modification to the contract (see page 1, of this report) five transistors were selected from an inventory of commercial transistors. A sixth transistor manufactured with a larger emitter area was also included. Each of the five was to meet the minimum engineering sample requirements. Discussion of this evaluation is contained in the following paragraphs.

B. Evaluation of the Five Additional Transistors

1. Table I, Subgroup 1 - Visual and Mechanical Inspections, Physical Dimensions

Commercial inventory contained only large finned transistors designated type P95200EE. The construction of these transistors is identical to the J15381 except each heat-pipe is fabricated from smooth tubing and the approximately four inch diameter fins are pressed and epoxied in place. Figure 28 illustrates the outline of this transistor.

2. Table I, Subgroup 2 - Electrical Charateristics

Table 24 lists a summary of results taken for the five devices using the Tektronix 576 curve tracer. Performance of these transistors was in excess of the Specification requirements for this group of tests.

3. Table I, Subgroup 3 - Thermal Resistance

Each of the five transistors were operated at a collector dissipation of 250 watts and a thermal resistance value was recorded for the junction to each heat-pipe surface. This data is summarized in Table 25 along with the results of the isothermal tests used to determine if the heat-pipes are functional. This ΔT value is the maximum temperature variation measured along each heat-pipe while the transistor is operated at about 250 watts dissipation. Normal measurement values do not exceed eight degrees. The thermal resistance value, measured at the base of a cooling fin, is slightly higher than that measured on the J15381 transistors and may be attributed to the epoxy interface.

OUTLINE DRAWING OF TRANSCALENT TRANSISTOR P95200EE

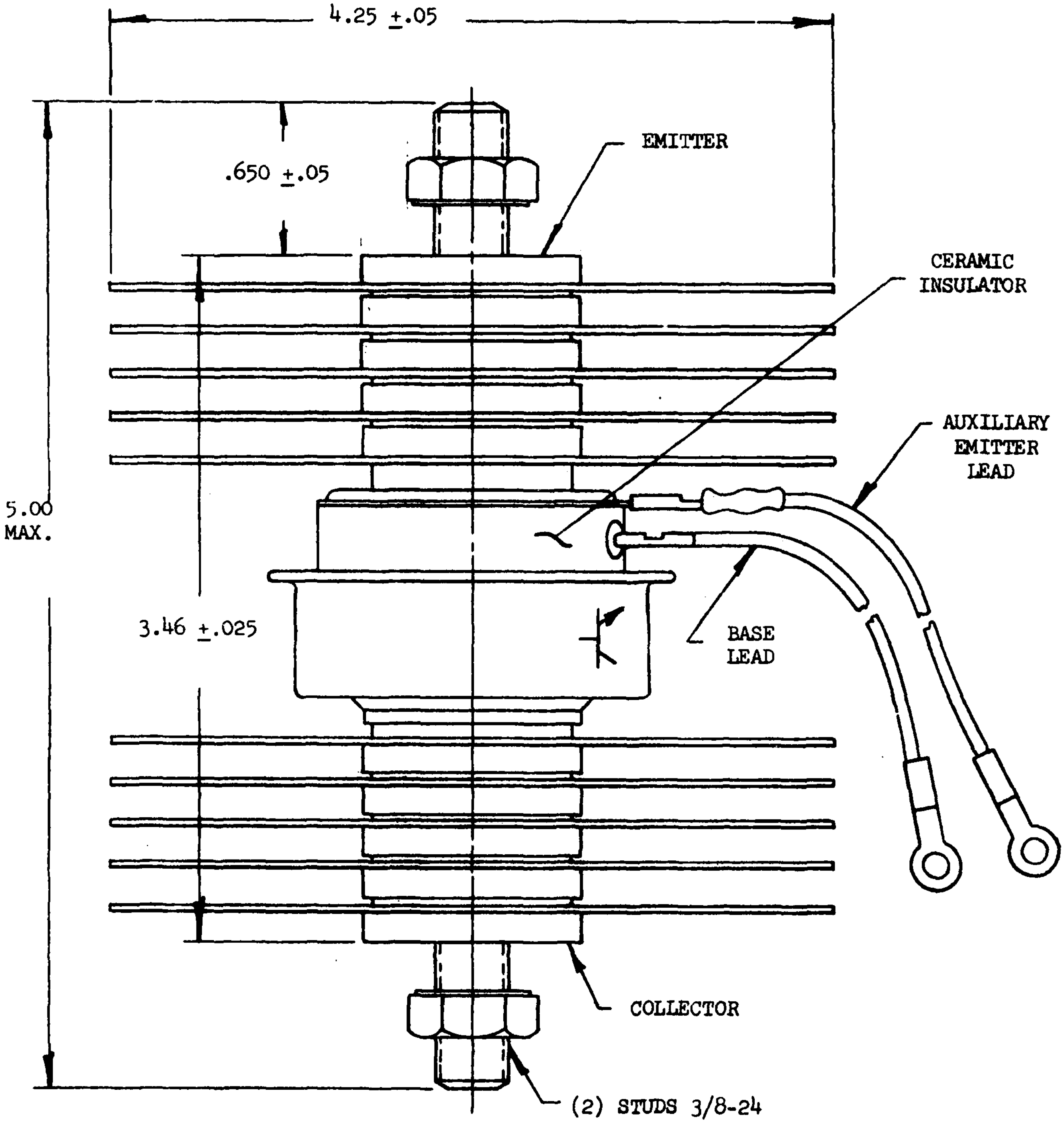


Figure 28

TABLE 24

Table I, Subgroup 2 Inspections of Additional Devices

Serial No.	Units	F135	F138	F141	F149	F150	Limits Min.	Limits Max.
I_{CEV} (750v)	ma	.35	.10	.30	.20	.10		15
I_{CEO} (350v)	ma	.20	.08	.30	.18	.08		20
I_{CBO}* (750v)	ma	.35	.11	.35	.20	.10		15
V_{EBO}	volts	10	10	10	10	10	8	
$h_{FE@10A}$ (V_{CE} = 5V)	--	27	45	34	35	48	20	
$h_{FE@100A}$ (V_{CE} = 5V)	--	8.8	9.3	9.6	8.5	8.4	--	--

*All Devices: V_{CBO} > 850 volts with currents less than 2 ma.

Table 25

Thermal Evaluation of P95200EE Transistors

Serial No.	$R_{\theta J\text{-}Coll}$ °C/W	$R_{\theta J\text{-}EMM}$ °C/W	ΔT, Coll °C	ΔT, EMM °C
F135	.16	.26	3.7	4.9
F138	.19	.27	4.7	5.0
F141	.15	.22	2.5	4.6
F149	.11	.21	4.6	3.8
F150	.11	.19	4.0	1.5

Test Conditions: V_{CE} = 5 Volts
I_C = 50 Amperes
Air Flow $\leq$ 150 CFM at 25°C Ambient

Specification Limit for Thermal Resistance is 0.4°C/watt maximum

4. Table II, Subgroup 1 - Forward Current Transfer Ratio, Saturation Voltage and Resistance

The forward current transfer ratio, h_{FE}, was measured during the thermal resistance tests. This is measured with D.C. conditions with the test parameters noted in Table 26. All five devices had current gains in excess of the minimum requirement of six times.

Table 26 also summarizes the Tektronix type 576 curve tracer measurements for the saturation voltage, V_{CE}(SAT). The base current may vary up to 20 amperes to meet the specification limit of a two volt maximum at a collector current of 50 amperes. The collector-to-emitter voltages were 0.5 volts or less. The saturation resistance is calculated from the quotient of the saturation voltage and the 50 ampere collector current. This information is also presented in Table 26.

C. Tests on the Transistor with Larger Emitter Area

An additional transister designated type J15492, S/N C178, is supplied to the preceding group of five. The construction is identical except that the emitter area was increased by about 20%. The peak current gain was 74 times at a collector voltage of five volts and 22 amperes. The gain at a collector current of 100 amperes was 13 times. This is, on the average, an increase over earlier devices, however, higher statistical samples should be used to determine the true effect of the increased area.

Voltage measurements were also optimistic as the collector-to-base voltage was 750 volts at 5 ma. leakage. The collector-to-emitter voltage (base open) reached 420 volts when tested with a curve tracer. The emitter-to-base voltage was 10 volts at 3.3 ma. leakage.

It sould be noted that of a number of transistor wafers constructed with this increased area this device had the highest collector-to-base leakage current and therfore may represent a worse case.

Thermal tests were not conducted with this device, however, the heat-pipes were tested for operation. At a collector-to-emitter voltage of 5.2 volts and a collector current of 23 amperes D.C. the differential temperature on the collector was 2.1°C and on the emitter was 0.9°C. The D.C. current gain at this level was 65 times.

Table 26

P95200EE Table II, S.G.1 Test Data

Parameter	Units	F135	F138	F141	F149	F150	Limits Min.	Limits Max.
		Serial Numbers						
h_{FE}*	-	10.7	11.8	15.6	11.0	15.0	6	
$V_{CE(SAT)}$	Volts	.45	.35	.5	.38	.38		2
$R_{CE(SAT)}$	MΩ	9	7	10	7.6	7.6		40

Test Conditions: Collector Current = 50 Amps.

*V_{CE} = 5.0 V.D.C.

Air flow $\leq$ 150 CFM, ambient air = 25°C

VII. DISCUSSION OF THE PROPOSED CONFIRMATORY SAMPLES

As a result of tests and of ideas formulated during the Engineering phase of this program, certain construction changes were proposed for later devices.

The major change in this proposal is the revised base terminal construction. Exernally this has resulted in a two piece ceramic insulator and a considerably more rugged base connection. Internally the base current path is more coaxial than the small wire used in prior devices and should result in low inductance value for this circuit.

A further advantage would be the assembly ease of the transistor. Present procedure requires that the base lead be soldered in place while the whole assembly is held rigid. Further, two circumferential welds must be made to complete the device. The new design uses contact fingers that mate with a cylindrical surface and finally a single circumferential weld to seal the transistor.

VIII. TEST EQUIPMENT DESCRIPTION

All of the electrical tests of the TABLE I and some of the tests of the TABLE II Inspections were carried out either using a commercial Tektronix Type 576 Curve Tracer, Figure 29, or the RCA designed and built Universal Transistor Test Equipment, Figure 30. The schematic diagram of this test set is shown in Figure 31. With the use of a line isolated oscilloscope, digital voltmeters and a surface temperature probe, various transistor characterization tests can be performed including the thermal resistance, the D.C. power dissipation, the D.C. forward current transfer ratio and other evaluations. Other specialized test circuits were designed and built for the pulse switching and second breakdown tests of the TABLE II Inspections.

TABLE III Inspections were performed in the existing test equipment form the thyristor MM&T Contract No. DAAB07-76-C-8120 as well as the RCA plant Environmental Laboratory equipment.

Operation of the Universal Transistor and the new test equipment built for this contract is described below.

A. Thermal Resistance Test Equipment

The V_{cc} supply in Figure 31 is adjusted to about seven volts D.C. With the air supply set at the desired volume, the V_h supply is adjusted to turn on the Device Under Test (DUT) at the required I_c. Then Q1 is pulsed into saturation at a low duty factor and V_M is adjusted (during this "off" period) to produce a low current level in the collector circuit that agrees with the calibration level to allow correlation between the junction temperature and the premeasured base-to-emitter calibration voltage. Thus, at high dissipation levels, the junction temperature can be monitored dynamically. The calibrating or measuring collector current used in these tests is preset at a 500 mA level.

B. Pulsed Switching Test Equipment

To reduce switching losses in tests requiring that the transistor switch between "on" saturation and a biased "off" condition, the circuit in Figures 32 and 33 was used. To implement this driver in the Universal Transistor Test Set, separate power supplies were used but the Hewlett-Packard Type 214A pulse generator output was rerouted to this new pulser's input and the base circuit switched entirely to the driver's output.

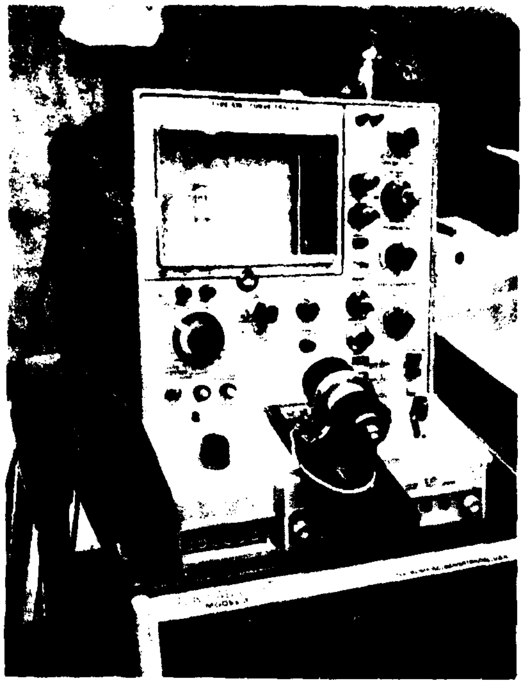


Figure 29 Tektronix Type 576 Curve Tracer and Fixture for Transcalent Transistor

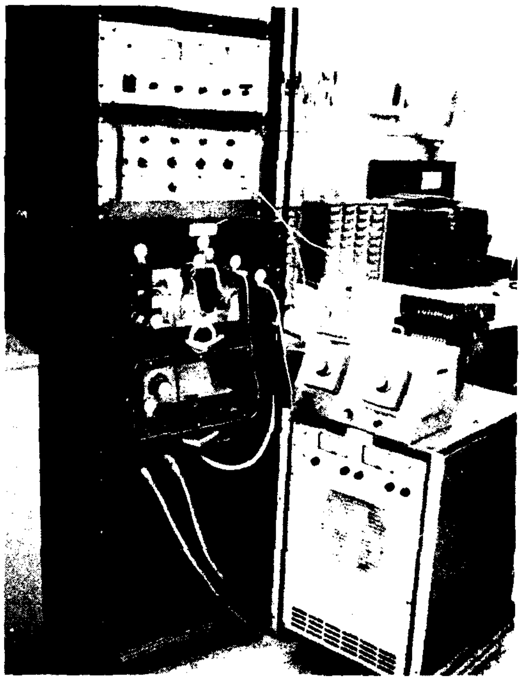
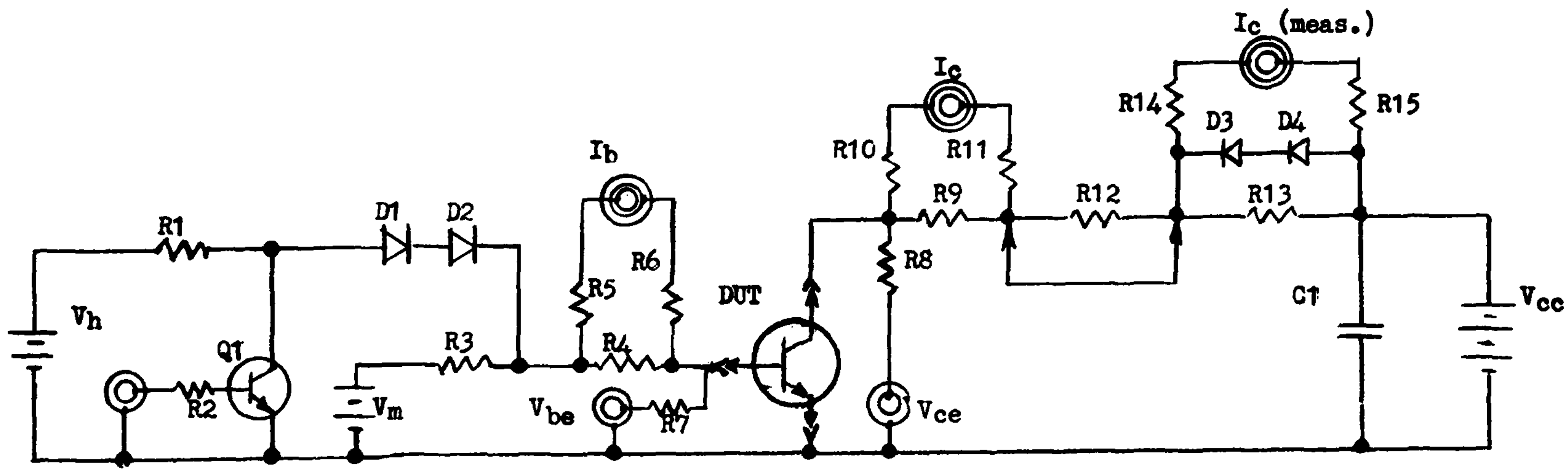


Figure 30 Transistor Universal Test Set with Regulated Power Supplies and Timer Cycling Equipment

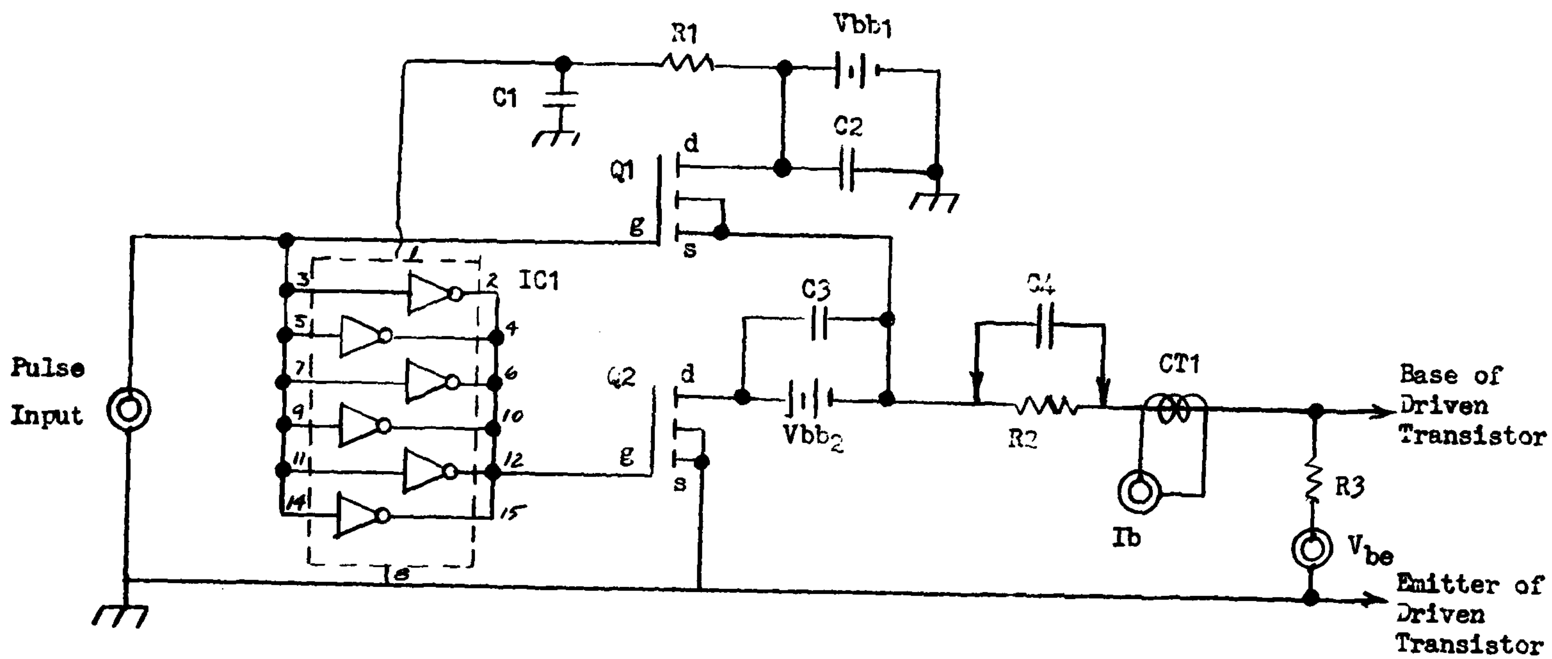


C1 1200 ufd.,400 V.d.c. Elect.Cap.
D1,D2 G.E. Type A96B Rectifier
D3,D4 G.E. Type A70B Rectifier
Q1 C2R Type GSDS50020 Transistor
V_{cc} Hewlett Packard Type 6475C Power Supply
0 -110 V.d.c., 0-100 A.d.c.
V_h Hewlett Packard Type 6268A Power Supply
0-40 V.d.c., 0-30 A.d.c.
V_m Hewlett Packard Type 6264B Power Supply
0-20 V.d.c., 0-20 A.d.c.

R1 1.6 Ohm, 50 W. Resistor
R2 10 Ohm, 2 W. Resistor
R3 700 Ohm, 50 W. Resistor
R4 0.001 Ohm Shunt Resistor
R5,R6 25 Ohm, $\frac{1}{4}$ W. Resistor
R7,R8 50 Ohm, $\frac{1}{4}$ W. Resistor
R9 0.001 Ohm Shunt Resistor
R10,R11 25 Ohm, $\frac{1}{4}$ W. Resistor
R12 6 Ohm, 5000 W. N.I.T. Resistor
R13 1 Ohm, 10 W. Resistor
R14,R15 25 Ohm, $\frac{1}{4}$ W. Resistor

Figure 31 RCA Transistor Test Equipment - Schematic

Figure 32   Power FET Driver



Pulse Input - 0 to 16 V. Pos. Pulse input from a Hewlett-Packard Type 214A Generator
C1 4 ufd., 50 V. Capacitor
C2 1500 ufd., 50 V. Capacitor
C3 100 ufd., 50 V. Capacitor
C4 4 ufd., 50 V. Capacitor(Base Current Peaking)
IC1 RCA Type CD4049B Hex Inverter
Q1, Q2 International Rectifier Type IRF130 HexFet Transistors
R1 100 Ohm, 2 W. Resistor
R2 0.5 Ohm, 10 W. Resistor(NIT)
CT1 Precision Current Transformer, Pearson Model 101, 1 Amp./Volt

Figure 33 Transistor Pulse Driver

With this circuit, switching tests could be performed without interaction between sources that supply the I_{b1} and I_{b2} forward and reverse base currents, respectively. The I_{b1} and I_{b2} currents then may be adjusted to be equal in amplitude, if desired. Voltage rise times of less than 50 nSec are available from this circuit with the current rise time limited only by the series inductive reactance of the base and collector circuit.

C. Forward Bias Second Breakdown Test Equipment

The circuit and its description is described fully in an RCA publication*. The block diagram of the equipment function is repeated in Figure 34. The circuit was modified only slightly from that in AN-6145 to increase the current capacity. The test equipment, shown in Figure 35, was then tested to 400 volts and 27 amperes at pulse widths up to 10 msec.

D. Reverse Bias Second Breakdown Test Equipment

The circuit used in this test is shown in Figure 36 and is described in MIL-STD-750B, Method 3053. The switch used is a type 2N6248 PNP transistor driven by a negative pulse from a Hewlett-Packard type 214A pulse generator. The prototype circuitry is shown assembled in Figure 37. The component values are listed in the specification with the exceptions noted in Section IV. C. 4. of this report.

E. Sustaining Voltage, Collector-to-Emitter Test Equipment

This circuit is similar to that used in the Reverse Bias Second Breakdown Test but with different component values. The transistor switch was also replaced by a mechanical snap-action type so that a true open circuit is used in the base circuit when the Device-Under-Test is switched off. The circuit diagram is shown in Figure 38. An oscilloscope is used with the horizontal amplifier attached to the voltage divider, reading V_{CE} and the vertical amplifier attached to the current monitoring resistor.

*RCA Application Note AN-6145, "A Test Set for Nondestructive Safe-Area Measurements Under High-Voltage, High-Current Conditions" by R. B. Jarl, 1973.

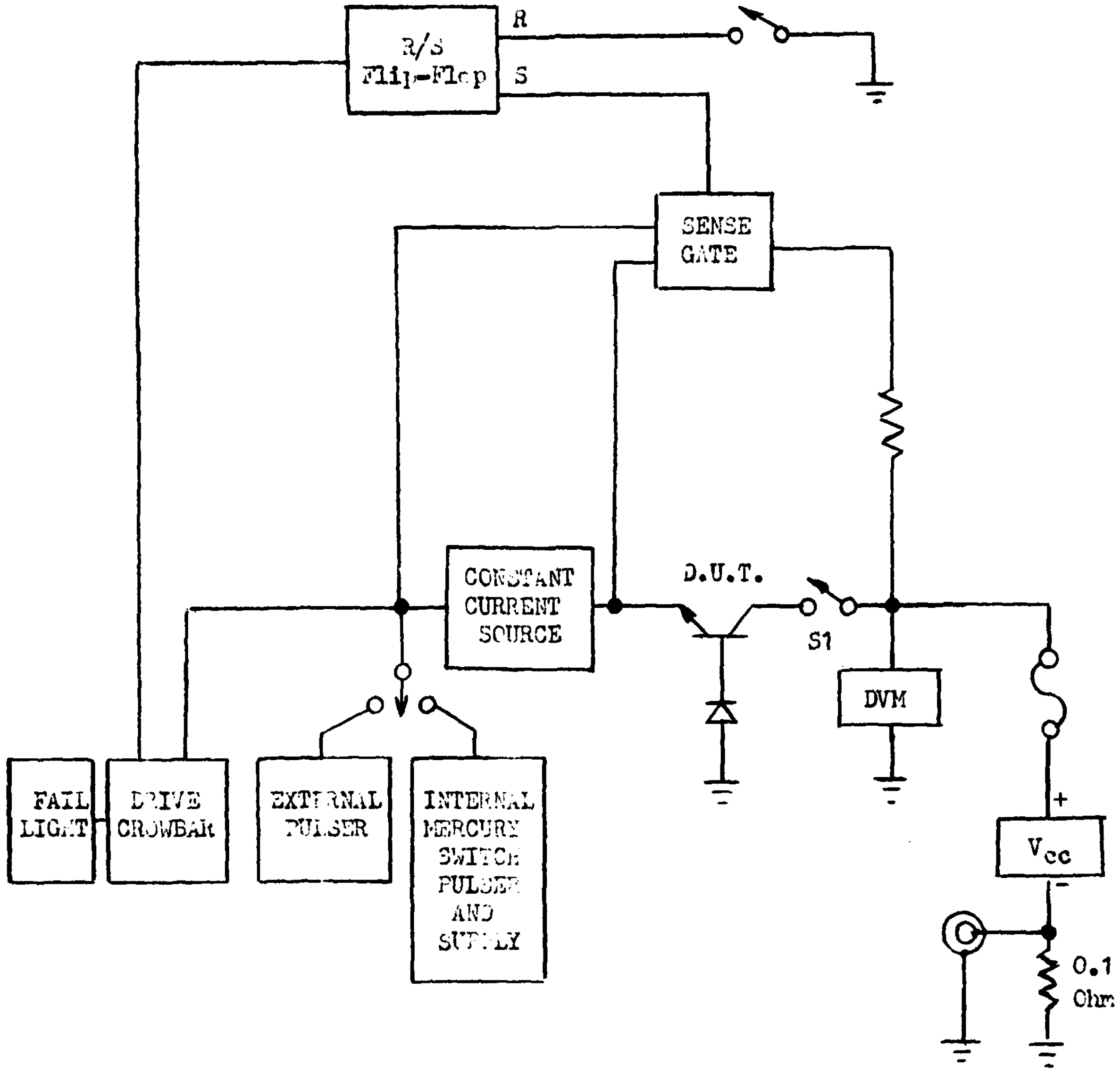


Figure 34 Forward Second Breakdown Test Equipment Block Diagram

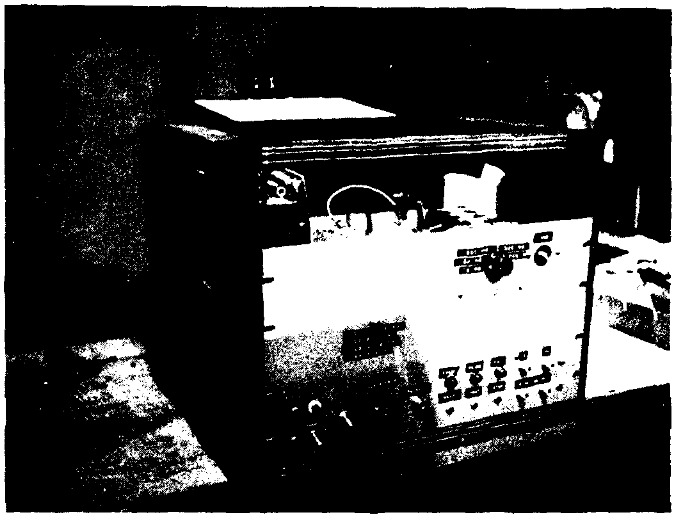
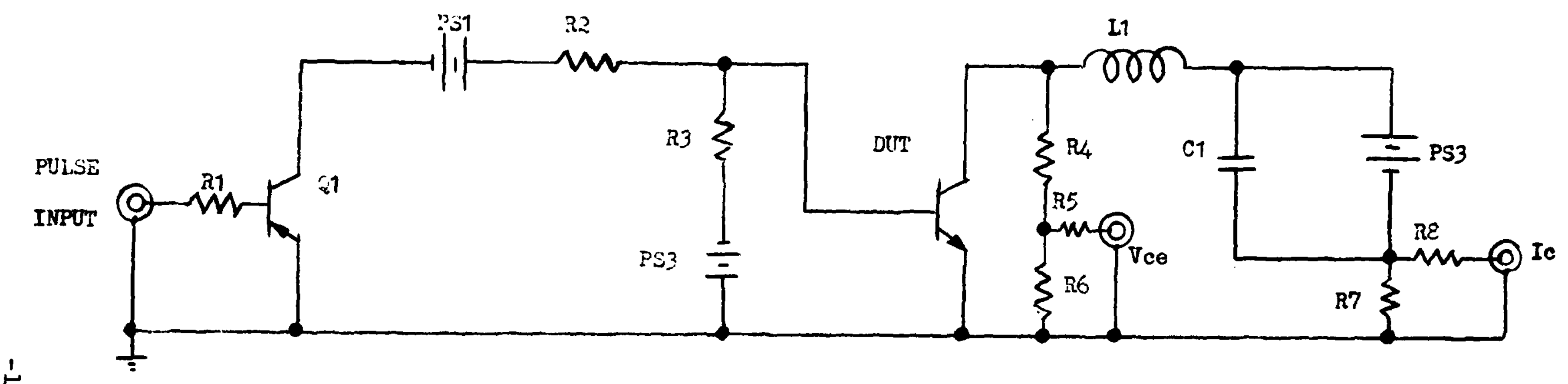


Figure 35 Forward Bias Second Breakdown Test Equipment



Pulse Input : 0 to -5 V. from Hewlett-Packard Type 214A Generator
C1 4000 ufd., 50 V. Capacitor
L1 Air-core inductor, 8 TPI, 9.75 in.lg., 1.75 in.dia., 0.058 in.dia.wire (48 uHy)
Q1 Type 2N6248 , PNP Transistor
R1 50 Ohm, 2W. Resistor
R2 10 Ohm, 4W. Resistor
R3 100 Ohm, 2W. Resistor
R4 1000 Ohm, 2W. Resistor
R5 50 Ohm, ½W. Resistor
R6 100 Ohm, ½W. Resistor
R7 0.043 Ohm, 1W. Resistor
R8 50 Ohm, ½W. Resistor

PS1 0-10 V.d.c., 1A. Power Supply
PS2 0-10 V.d.c., 0.1A. Power Supply
PS3 0-24 V.d.c., 100 A. Power Supply

Figure 36 Reverse Bias Second Breakdown Test Circuit

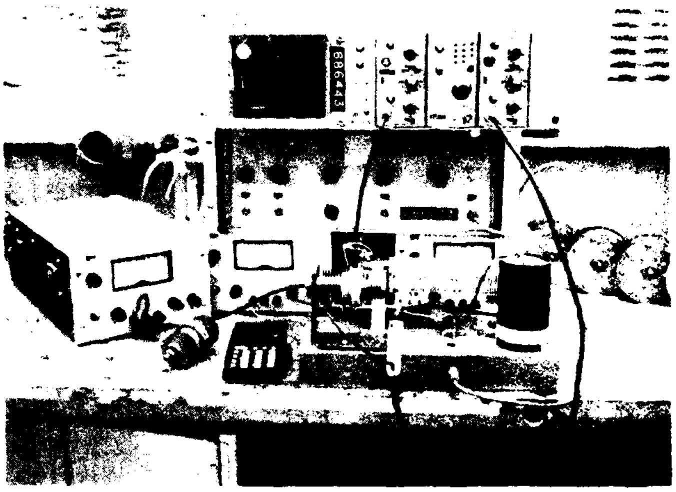
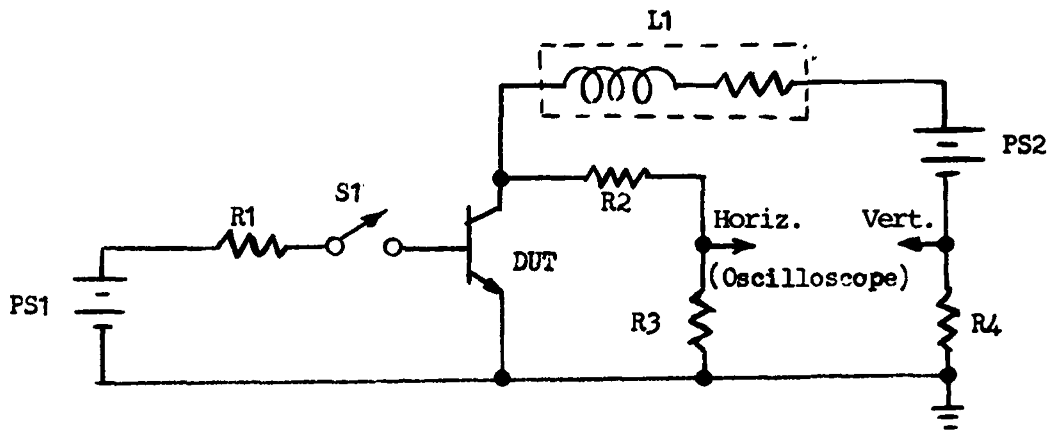


Figure 37 Reverse Bias Second Breakdown Test (Prototype)



L1 10 milli-Hy.Choke, .11 Ohm Resistance, Stancor Type C-2688
PS1 0 to 10 V.d.c., .1 A. Power Supply
PS2 0 to 10 V.d.c., 10 A. Power Supply
R1 200 Ohm, 2W. Resistor
R2 1000 Ohm, 1W. Resistor
R3 10 Ohm, $\frac{1}{2}$W. Resistor
R4 0.196 Ohm, $\frac{1}{2}$W. Resistor
S1 SPST Snap Action Switch

Figure 38 $V_{CEO(sus)}$ Test Circuit

To test a transistor, the Collector-to-Emitter voltage (PS2) is set to eight volts and the Base-to-Emitter voltage (PS1) is set to zero volts with the switch (S1) closed. The PS1 supply is then raised to produce some collector current. When S1 is opened, the switching locus on the oscilloscope is observed for the voltage peak. The process is repeated, elevating the voltage from PS1 incrementally until the characteristic flattening of the voltage pulse is observed. The limit of voltage is read at a particular current level. In this case, one ampere of collector current is used.

F. Table III Test Equipment

Figures 39 through 45 show the various test equipments used in the environmental testing for the Table III requirements. The equipment for Subgroup 4, Thermal Fatigue Test, is not shown since it is incorporated in the Universal Test Set of Figure 30.

G. Test Equipment Calibration

Equipments involved in the measurement of parameters listed as maximum or minimum limits as well as those listed in the specific conditions of the tests are calibrated at four to six months intervals. A computer call-out system is used; issuing the reminder and requiring verification that the work is complete. The calibration is carried out by the RCA Meter Laboratory Calibration and Standard Department. Environmental test equipment calibrations in the RCA-Lancaster Environmental Laboratory are also performed at four to six months intervals.

Figure 39 Reduced Barometric Pressure Test Equipment (Vacuum Bell Shown without Safety Enclosure)

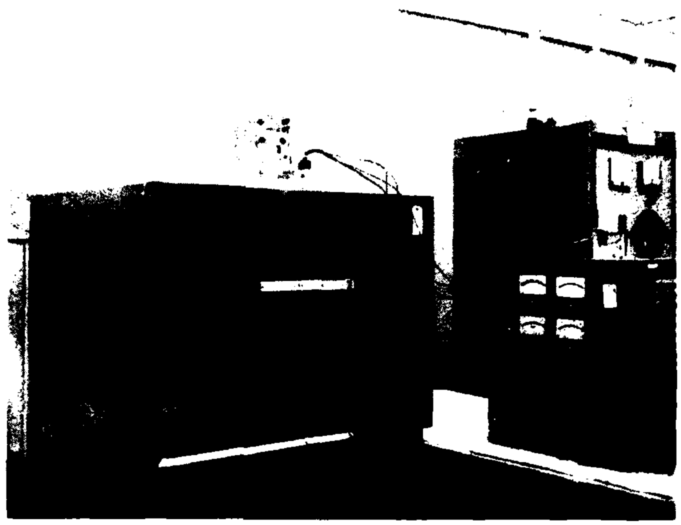


Figure 40 Blocking Voltage Life Test Set, Including the Temperature Controlled Oven and Regulated Power Supplies

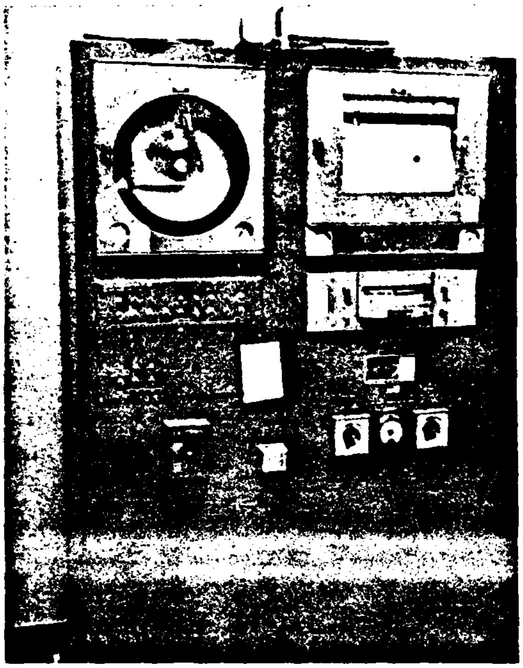


Figure 41a

Figure 41b

American Research Corp. Temperature-Altitude Chamber

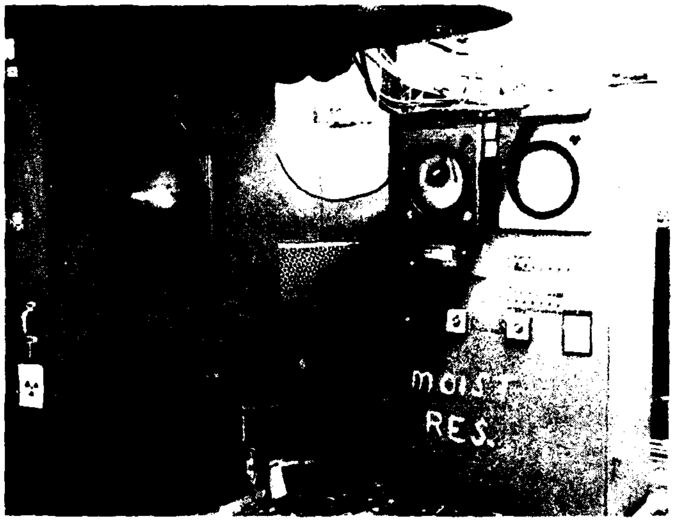


Figure 42   Moisture Resistance Test Equipment

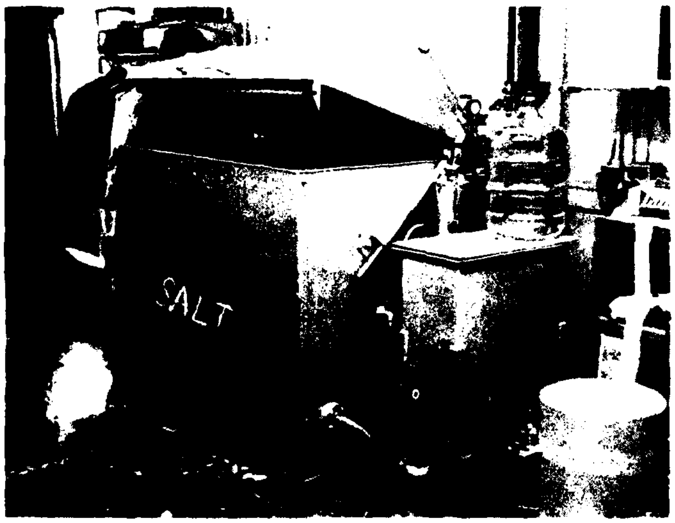


Figure 43   Salt Spray Test Equipment

Figure 44 Barry Varipulse Shock Machine

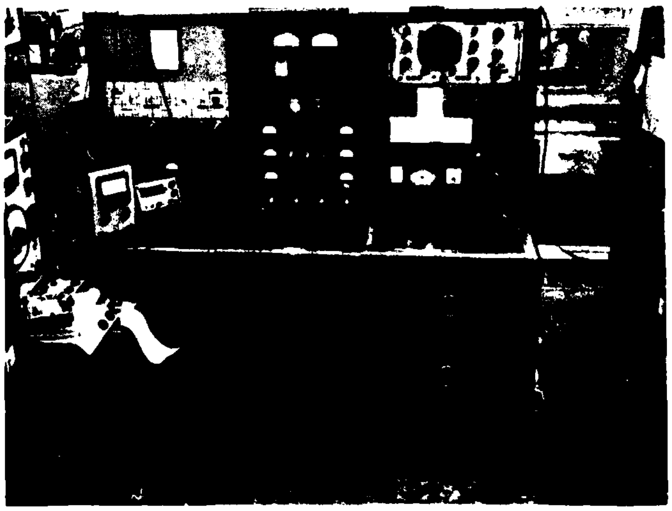


Figure 45a Figure 45b

7,000 Pound Ling Vibrator and Controls

IX. CONCLUSIONS AND RECOMMENDATIONS

A. Program Evaluation and Review Technique

A program Evaluation and Review Technique (PERT) chart was prepared and submitted early in the program in accordance with the DD 1423. This chart contained the objectives for all major portions of the contract along with the most critical path and delivery dates for all items. Although the scope of this contract has been drastically reduced, the PERT chart is included as a reference item. The chart is reporduced in Figure 46.

B. Recommendations for Subsequent Inspections

From the data obtained in the test of the ten Engineering Sample transistors, the following changes or corrections to the Specification are recommended:

1. Page 3, Section 4.3 - Engineering Test Sample Inspection

   a. TABLE II, Subgroup 2 should be TABLE I, Subgroup 2 to comply with the group of tests listed.

   b. The temperature points, T_C, should be moved on the drawing from the right side of the heat-pipes to the left side so that case temperature measurements are taken on the down-wind side of the device.

2. Figure 2 - Basic Circuit for Breakdown Life Test

   a. A plus sign should be placed on the upper side of the one-half wave A.C. supply to indicate correct polarity.

   b. Each Test Cell should indicate a base-to-emitter short to comply with the required Bias Condition C.

3. TABLE I - Group A Inspection - Subgroup 2

   a. It is recommended that the "Collector-to-Emitter Cutoff Current with Base Reverse Biased" test be deleted since the test voltage is the same as in the "Collector-to-Base Cutoff Current" test. The same junction is evaluated in both tests.

   b. The "Collector-to-Emitter Cutoff Current with Base Open" test should be changed to a sustaining voltage test, $V_{CEO(sus)}$ and should be described as: "Collector-to-Emitter Sustaining voltage with Base Open" using the circuit of Method 3053 and the Details as follows:

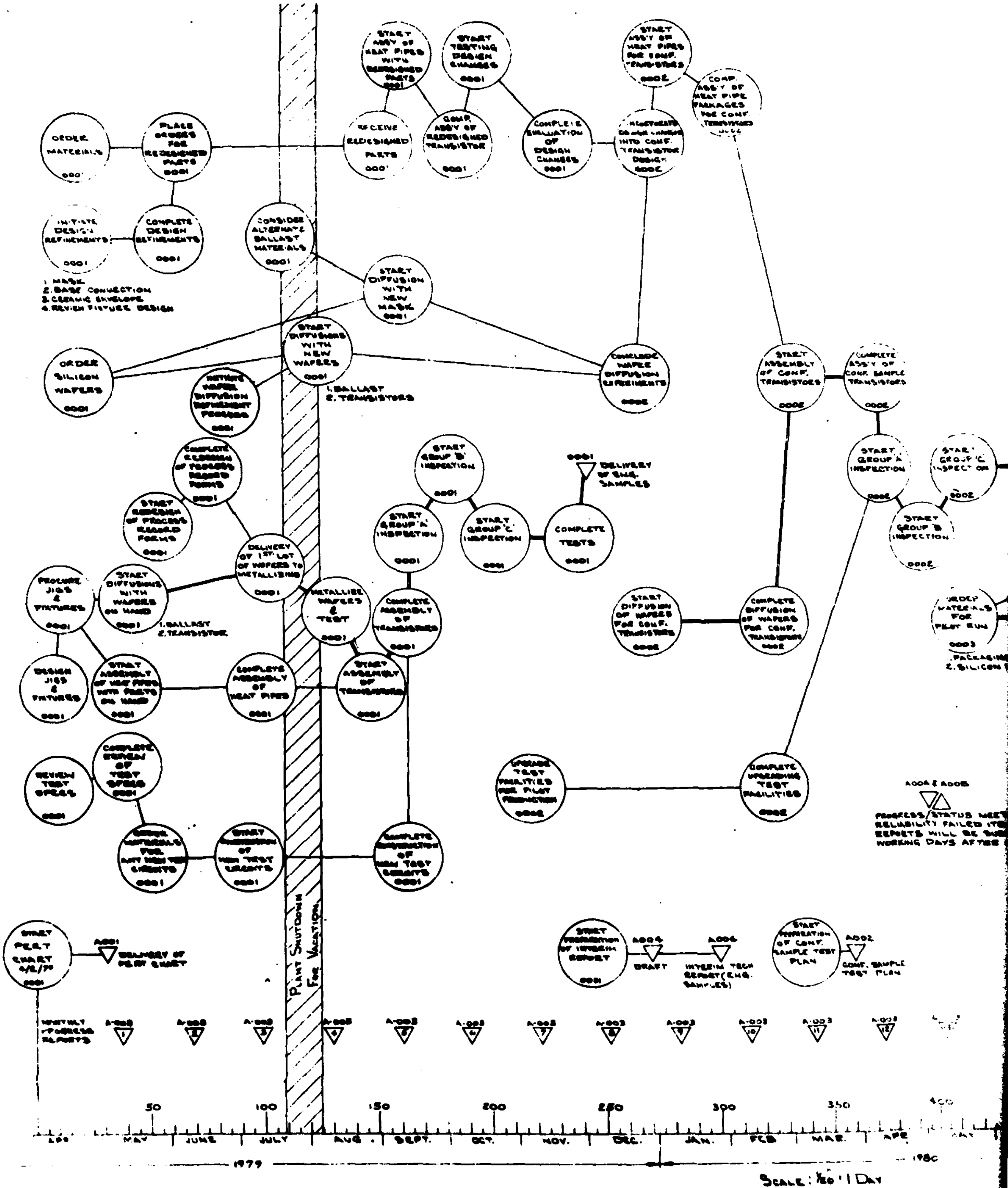

ORDER MATERIALS 0001
PLACE ORDERS FOR REDESIGNED PARTS 0001
INITIATE DESIGN REFINEMENTS 0001
COMPLETE DESIGN REFINEMENTS 0001
1. MASK
2. BASE CONNECTION
3. CERAMIC ENVELOPE
4. REVIEW FIXTURE DESIGN
CONSIDER ALTERNATE BALLAST MATERIALS 0001
RECEIVE REDESIGNED PARTS 0001
START ASS'Y OF HEAT PIPES WITH REDESIGNED PARTS 0001
COMP. ASS'Y OF REDESIGNED TRANSISTOR 0001
START TESTING DESIGN CHANGES 0001
COMPLETE EVALUATION OF DESIGN CHANGES 0001
START ASS'Y OF HEAT PIPES FOR CONF. TRANSISTORS 0002
COMP. ASS'Y OF HEAT PIPE PACKAGES FOR CONF TRANSISTORS 0002
INTO CONF. TRANSISTOR DESIGN 0002
START DIFFUSION WITH NEW MASK 0001
ORDER SILICON WAFERS 0001
START DIFFUSIONS WITH NEW WAFERS 0001
1. BALLAST
2. TRANSISTORS
INITIATE WAFER DIFFUSION REFINEMENT PROCESS 0001
CONCLUDE WAFER DIFFUSION EXPERIMENTS 0002
START ASSEMBLY OF CONF. TRANSISTORS 0002
COMPLETE ASS'Y OF CONF. SAMPLE TRANSISTORS 0002
START GROUP A INSPECTION 0002
START GROUP C INSPECTION 0002
START GROUP B INSPECTION 0002
ORDER MATERIALS FOR PILOT RUN 0003
1. PACKAGING
2. SILICON
START REDESIGN OF PROCESS RECORD FORMS 0001
DELIVERY OF 1ST LOT OF WAFERS TO METALLIZING 0001
PROCURE JIGS & FIXTURES 0001
START DIFFUSIONS WITH WAFERS ON HAND 0001
1. BALLAST
2. TRANSISTOR
DESIGN JIGS & FIXTURES 0001
START ASSEMBLY OF HEAT PIPES WITH PARTS ON HAND 0001
COMPLETE ASSEMBLY OF HEAT PIPES 0001
METALLIZE WAFERS & TEST 0001
START ASSEMBLY OF TRANSISTORS
COMPLETE ASSEMBLY OF TRANSISTORS 0001
START GROUP 'A' INSPECTION 0001
START GROUP 'B' INSPECTION 0001
START GROUP 'C' INSPECTION 0001
COMPLETE TESTS 0001
0001 DELIVERY OF ENG. SAMPLES
START DIFFUSION OF WAFERS FOR CONF. TRANSISTORS 0002
COMPLETE DIFFUSION OF WAFERS FOR CONF. TRANSISTORS 0002
REVIEW TEST SPECS 0001
COMPLETE REVIEW OF TEST SPECS 0001
START FABRICATION OF NEW TEST CIRCUITS 0001
COMPLETE FABRICATION OF NEW TEST CIRCUITS 0001
UPGRADE TEST FACILITIES FOR PILOT PRODUCTION 0002
COMPLETE UPGRADING TEST FACILITIES 0002
A00A & A00B
PROGRESS/STATUS MEET
RELIABILITY FAILED ITE
REPORTS WILL BE SUB
WORKING DAYS AFTER
START PERT CHART 4/2/79 0001
A001 DELIVERY OF PERT CHART
PLANT SHUTDOWN FOR VACATION
START PREPARATION OF INTERIM REPORT 0001
A004 DRAFT
A004 INTERIM TECH REPORT (ENG. SAMPLES)
START PREPARATION OF CONF. SAMPLE TEST PLAN
A002 CONF. SAMPLE TEST PLAN
MONTHLY PROGRESS REPORTS
A-003
50
100
150
200
250
300
350
400
APR
MAY
JUNE
JULY
AUG.
SEPT.
OCT.
NOV.
DEC.
JAN.
FEB
MAR.
APR
1979
1980
SCALE: 1/20" : 1 DAY

Figure 46

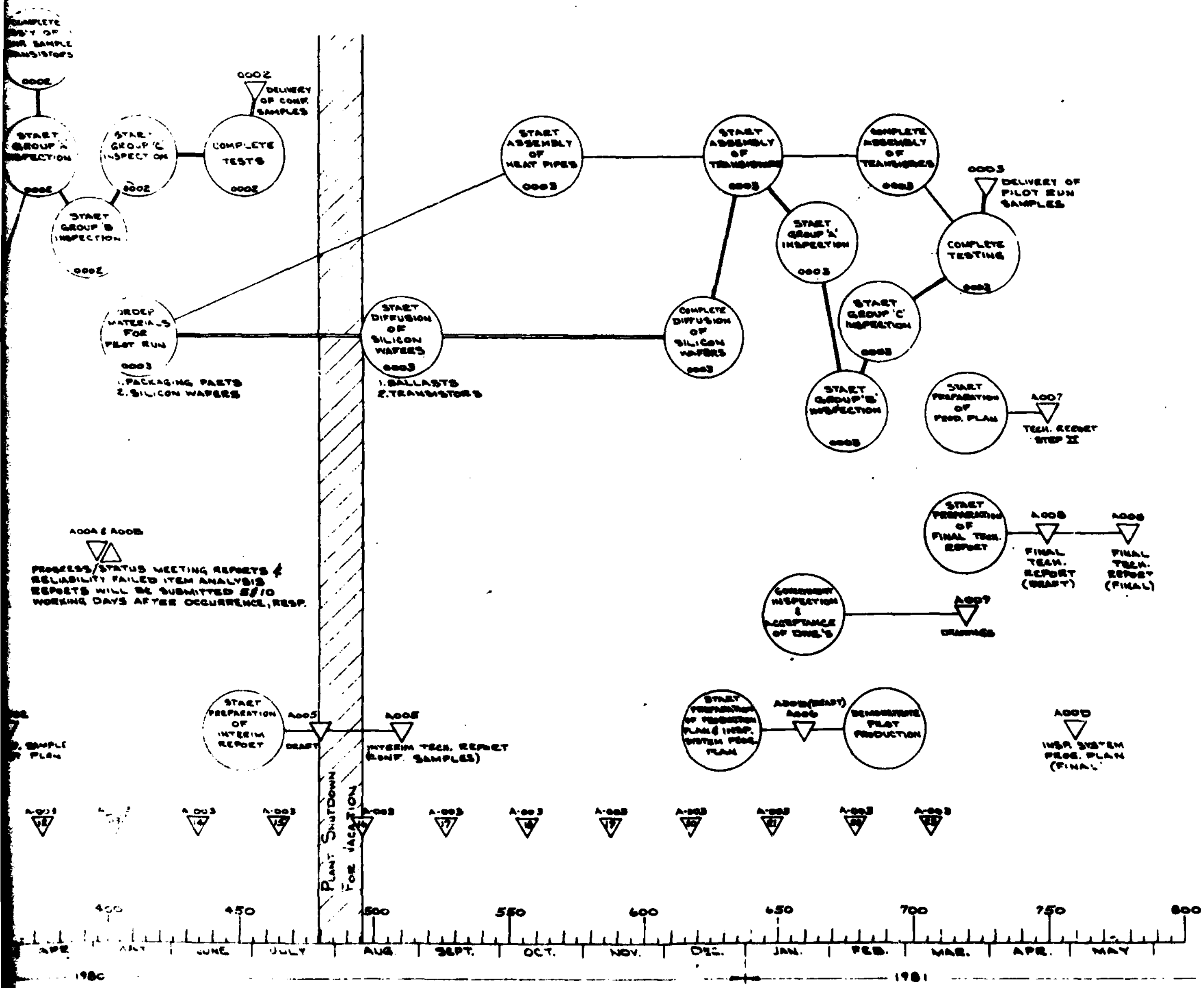


Figure 46

RCA

PERT CHART

CONTRACT: DAAK 70-79-C-0019

PREPARED BY:

DRAWN BY:

APPROVED BY:

V_{CC} = 8 V, I_C = 1 Amp., $R_{BB} = \infty$
V_{BB1} = 0 to 10 V, R_{BB1} = 10 Ω Load
Condition C, L = 10 mHy, R of inductor
<0.5 Ω, R_s <0.5 Ω

The symbol becomes $V_{CEO(sus)}$ and the limit should be 350 volts, minimum.

4. TABLE II - Group B Inspection, Subgroup 1

   a. Statistical analysis of the data of this report and results of investigations of similar devices support the change of the "Forward-Current Transfer Ratio" test from a minimum of 10 to a minimum of 6. This was recommended also in DP 8165.

5. TABLE II - Group B Inspection, Subgroup 4

   a. From the results of experimentation, the details of this test should be altered to read as follows:

      Load condition C, unclamped inductive load;
      L = 48 μhy, Q> 5 @ 1 KHz, duty cycle >1.8%
      Base drive pulse width = 300 μs;
      R_{BB1} = 10 Ω, V_{BB1} = 0-10 V, I_C = 50 A,
      V_{CC} = 10 V, V_{BB2} = -1.5V, R_{BB} = 100 Ω
      R_s = 0.05 Ω.

6. TABLE III - Group C Inspection, Subgroup 2

   Under Details: "Peak Value of V_{CEO} = " should read "Peak Value of V_{CE} = " since the base is not open circuited as the subscript "0" signifies. "Bias Condition C" describes a short circuit base-to-emitter for this test.

No other changes are anticipated, however, an area of concern related to device performance is the thermal shock test which resulted in a reduction of emitter-to-base voltage holdoff in one device. This device still meets the specification limit, however.

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